LP2985-N 采用 SOT-23 封装的 150mA、低噪声、低功耗、超低压降稳压器

1 特性

- V_{IN} 范围：2.5V 至 16V
- V_{OUT} 范围（新芯片）：
  - 1.2V 至 5.0V（固定值，100mV 阶跃）
- V_{OUT} 范围（旧芯片）：2.5V 至 6.1V
- V_{OUT} 精度：
  - A 级旧芯片为 ±1%
  - 标准级旧芯片为 ±1.5%
  - ±0.5%（仅限新芯片）
- 在整个负载和温度范围内的输出精度：
  - ±1%（新芯片）
- 输出电流：高达 150mA
- 低 I_Q（新芯片）：I_{LOAD} = 0mA 时为 71μA
- 低 I_Q（新芯片）：I_{LOAD} = 150mA 时为 750μA
- 关断电流：
  - 旧芯片为 0.05μA（典型值）
  - 新芯片为 1.12μA（典型值）
- 低噪声：30μV_{RMS}，带 10nF 旁路电容器
- 输出电流限制和热保护
- 使用 2.2μF 陶瓷电容器实现稳定工作
- 高 PSRR：1kHz 频率下为 70dB，1MHz 频率下为 40dB
- 工作结温：–40°C 至 +125°C
- 封装：5 引脚 SOT-23 (DBV) 超低压降电压

2 应用

- 洗衣机和烘干机
- 陆地移动无线电
- 有源天线系统 mMIMO
- 无线电动工具
- 电机驱动器和控制板

3 说明

LP2985-N 是一款宽输入、固定输出、低噪声、低压降稳压器，支持 2.5V 至 16V 的输入电压范围和高达 150mA 的负载电流。LP2985-N 支持 1.2V 至 5.0V（新芯片）和 2.5V 至 6.1V（旧芯片）的输出范围。

此外，LP2985-N（新芯片）在整个负载和温度范围内具有 1% 的输出精度，可满足低压微控制器 (MCU) 和处理器的需求。

30μV_{RMS} 的低输出噪声（带 10nF 旁路电容器）以及 1kHz 时大于 70dB 和 1MHz 时大于 40dB 的宽带宽 PSRR 性能有助于衰减上游直流/直流转换器的开关频率，并尽可能减少后置稳压器滤波。

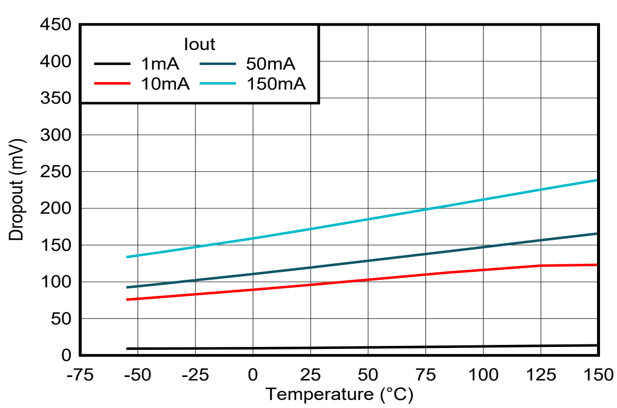
内部软启动时间和电流限制保护可减小启动期间的浪涌电流，从而尽可能降低输入电容。还包括标准保护特性，例如过流和过热保护。

LP2985-N 采用 5 引脚、2.9mm × 1.6mm SOT-23 (DBV) 封装。

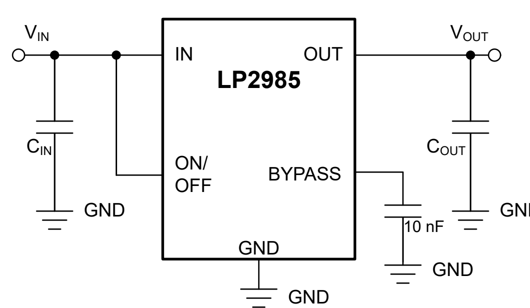
封装信息

器件型号	封装(1)	封装尺寸(2)
LP2985-N	DBV（SOT-23，5）	2.9 mm × 2.8 mm

(1) 如需了解所有可用封装，请参阅数据表末尾的可订购产品附录。
(2) 封装尺寸（长 x 宽）为标称值，并包括引脚（如适用）。



新芯片的压降电压与温度间的关系



典型应用电路

English Data Sheet: SNVS018

Table of Contents

4 Revision History

注：以前版本的页码可能与当前版本的页码不同

Changes from Revision Z (May 2023) to Revision AA (July 2023)	Page
• Widening IGND spec limits to accommodate complete VOUT range	5

Changes from Revision Y (December 2016) to Revision Z (May 2023)	Page
• 向文档添加了 M3 后缀器件	1
• 更改了整个文档以与新格式保持一致，并更新了 LDO 特性、功能和应用的详细说明	1
• 添加了指向*应用* 部分的链接	1
• Added M3-suffix (new chip) curves to *Typical Characteristics* section	9
• Added *Block Diagram for New Chip* to *Functional Block Diagrams* section	15
• Added M3-suffix (new chip) curves to *Application Curves* section	23

5 Pin Configuration and Functions

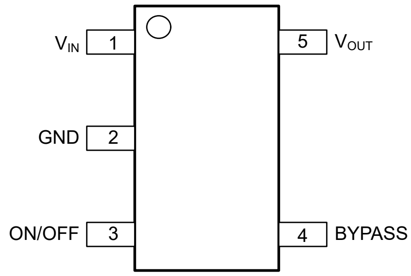


图 5-1. DBV Package, 5-Pin SOT-23 (Top View)

表 5-1. Pin Functions

PIN		TYPE	DESCRIPTION
NAME	NO.		
BYPASS	4	I/O	BYPASS pin to achieve low noise performance. Connecting an external capacitor between the BYPASS pin and ground reduces reference voltage noise. See the *Recommended Operating Conditions* section for more information.
GND	2	—	Ground
ON/OFF	3	I	Enable pin for the LDO. Driving the ON/OFF pin high enables the device. Driving this pin low disables the device. High and low thresholds are listed in the *Electrical Characteristics* table. Tie this pin to V_{IN} if unused.
V_{IN}	1	I	Input supply pin. Use a capacitor with a value of 1 μF or larger from this pin to ground. See the *Input and Output Capacitor Requirements* section for more information.
V_{OUT}	5	O	Output of the regulator. Use a capacitor with a value of 2.2 μF or larger from this pin to ground.[1] See the *Input and Output Capacitor Requirements* section for more information.

(1) The nominal output capacitance must be greater than 2.2 μF. Throughout this document, the nominal derating on these capacitors is 50%. Make sure that the effective capacitance at the pin is greater than 1 μF.

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)[(1)] [(2)]

		MIN	MAX	UNIT
V_{IN}	Continuous input voltage range (for legacy chip)	–0.3	16	V
	Continuous input voltage range (for new chip)	–0.3	18	
V_{OUT}	Output voltage range (for legacy chip)	–0.3	9	
	Output voltage range (for new chip)	–0.3	V_{IN} + 0.3 or 9 (whichever is smaller)	
V_{BYPASS}	BYPASS pin voltage range (for new chip)	–0.3	3	
$V_{ON/\overline{OFF}}$	ON/$\overline{\text{OFF}}$ pin voltage range (for legacy chip)	–0.3	16	
	ON/$\overline{\text{OFF}}$ pin voltage range (for new chip)	–0.3	18	
Current	Maximum output	Internally limited		A
Temperature	Operating junction, T_J	–55	150	°C
	Storage, T_{stg}	–65	150	

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltages with respect to GND.

6.2 ESD Ratings

			VALUE (Legacy Chip)	VALUE (New Chip)	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001[(1)]	±2000	±3000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101[(2)]	±500	±1000	

(1) JEDEC document JEP155 states that 2-kV HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 500-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

		MIN	NOM	MAX	UNIT
V_{IN}	Supply input voltage (for legacy chip)	2.2		16	V
	Supply input voltage (for new chip)	2.5		16	
V_{OUT}	Output voltage (for legacy chip)	1.2		10.0	
	Output voltage (for new chip)	1.2		5.0	
V_{BYPASS}	Bypass voltage		1.2		
$V_{ON/\overline{OFF}}$	Enable voltage (for legacy chip)	0		V_{IN}	
	Enable voltage (for new chip)	0		16	
I_{OUT}	Output current	0		150	mA
C_{IN} [(2)] [(1)]	Input capacitor		1		µF
C_{OUT}	Output capacitor (for legacy chip)	2.2	4.7		µF
	Output capacitance (for new chip) [(1)]	1	2.2	200	
T_J	Operating junction temperature	–40		125	°C

(1) All capacitor values are assumed to derate to 50% of the nominal capacitor value. Maintain an effective output capacitance of 1 µF minimum for stability.
(2) Minimum input capacitor of 2.2 µF is recquired if the source impedance is more than 0.5 Ω.

6.4 Thermal Information

THERMAL METRIC (2) (1)		Legacy Chip DBV (SOT23-5) 5 PINS	New Chip DBV (SOT23-5) 5 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	205.4	178.6	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	78.8	77.9	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	46.7	47.2	°C/W
ψ_{JT}	Junction-to-top characterization parameter	8.3	15.9	°C/W
ψ_{JB}	Junction-to-board characterization parameter	46.3	46.9	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application note.
(2) Thermal performance results are based on the JEDEC standard of 2s2p PCB configuration. These thermal metric parameters can be further improved by 35-55% based on thermally optimized PCB layout designs. See the analysis of the Impact of board layout on LDO thermal performance application report.

6.5 Electrical Characteristics

specified at T_J = 25°C, V_{IN} = $V_{OUT(nom)}$ + 1.0 V or VIN = 2.5 V (whichever is greater), I_{OUT} = 1 mA, $V_{ON/OFF}$ = 2 V, C_{IN} = 1.0 µF, and C_{OUT} = 2.2 µF (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
ΔV_{OUT}	Output voltage tolerance	I_L = 1 mA	Legacy chip (standard grade)	−1.5		1.5	%
			Legacy chip (A grade)	−1.0		1.0	
			New chip	−0.5		0.5	
		1 mA ≤ I_L ≤ 50 mA	Legacy chip (standard grade)	−2.5		2.5	
			Legacy chip (A grade)	−1.5		1.5	
			New chip	−0.5		0.5	
		1 mA ≤ I_L ≤ 150 mA	Legacy chip (standard grade)	−3.0		3.0	
			Legacy chip (A grade)	−2.5		2.5	
			New chip	−0.5		0.5	
		1 mA ≤ I_L ≤ 50 mA, −40°C ≤ T_J ≤ 125°C	Legacy chip (standard grade)	−3.5		3.5	
			Legacy chip (A grade)	−2.5		2.5	
			New chip	−1		1	
		1 mA ≤ I_L ≤ 150 mA, −40°C ≤ T_J ≤ 125°C	Legacy chip (standard grade)	−4.0		4.0	
			Legacy chip (A grade)	−3.5		3.5	
			New chip	−1		1	

6.5 Electrical Characteristics (continued)

specified at T_J = 25°C, V_{IN} = $V_{OUT(nom)}$ + 1.0 V or VIN = 2.5 V (whichever is greater), I_{OUT} = 1 mA, $V_{ON/OFF}$ = 2 V, C_{IN} = 1.0 µF, and C_{OUT} = 2.2 µF (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
$\Delta V_{OUT(\Delta VIN)}$	Line regulation	$V_{O(NOM)}$ + 1 V ≤ V_{IN} ≤ 16 V	Legacy chip		0.007	0.014	%/V
			New chip		0.002	0.014	
		$V_{O(NOM)}$ + 1 V ≤ V_{IN} ≤ 16 V, –40°C ≤ T_J ≤ 125°C	Legacy chip		0.007	0.032	
			New chip		0.002	0.032	
V_{IN} - V_{OUT}	Dropout voltage[(1)]	I_{OUT} = 0 mA	Legacy chip		1	3	mV
			New chip		1	2.75	
		I_{OUT} = 0 mA, –40°C ≤ T_J ≤ 125°C	Legacy chip			5	
			New chip			3	
		I_{OUT} = 1 mA	Legacy chip		7	10	
			New chip		11.5	14	
		I_{OUT} = 1 mA, –40°C ≤ T_J ≤ 125°C	Legacy chip			15	
			New chip			17	
		I_{OUT} = 10 mA	Legacy chip		40	60	
			New chip		98	115	
		I_{OUT} = 10 mA, –40°C ≤ T_J ≤ 125°C	Legacy chip			90	
			New chip			148	
		I_{OUT} = 50 mA	Legacy chip		120	150	
			New chip		120	145	
		I_{OUT} = 50 mA, –40°C ≤ T_J ≤ 125°C	Legacy chip			225	
			New chip			184	
		I_{OUT} = 150 mA	Legacy chip		280	350	
			New chip		180	198	
		I_{OUT} = 150 mA, –40°C ≤ T_J ≤ 125°C	Legacy chip			575	
			New chip			254	

6.5 Electrical Characteristics (continued)

specified at T_J = 25°C, V_{IN} = $V_{OUT(nom)}$ + 1.0 V or VIN = 2.5 V (whichever is greater), I_{OUT} = 1 mA, $V_{ON/OFF}$ = 2 V, C_{IN} = 1.0 µF, and C_{OUT} = 2.2 µF (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
I_{GND}	GND pin current	I_{OUT} = 0 mA	Legacy chip		65	95	µA
			New chip		69	95	
		I_{OUT} = 0 mA, –40°C ≤ T_J ≤ 125°C	Legacy chip			125	
			New chip			123	
		I_{OUT} = 1 mA	Legacy chip		75	110	
			New chip		78	110	
		I_{OUT} = 1 mA, –40°C ≤ T_J ≤ 125°C	Legacy chip			170	
			New chip			140	
		I_{OUT} = 10 mA	Legacy chip		120	220	
			New chip		175	210	
		I_{OUT} = 10 mA, –40°C ≤ T_J ≤ 125°C	Legacy chip			400	
			New chip			250	
		I_{OUT} = 50 mA	Legacy chip		350	600	
			New chip		380	440	
		I_{OUT} = 50 mA, –40°C ≤ T_J ≤ 125°C	Legacy chip			900	
			New chip			650	
		I_{OUT} = 150 mA	Legacy chip		850	1200	
			New chip		765	890	
		I_{OUT} = 150 mA, –40°C ≤ T_J ≤ 125°C	Legacy chip			2000	
			New chip			1060	
		$V_{ON/OFF}$ < 0.3 V, V_{IN} = 16 V	Legacy chip		0.01	0.08	
			New chip		1.25	1.75	
		$V_{ON/OFF}$ < 0.15 V, V_{IN} = 16 V, –40°C ≤ T_J ≤ 85°C	Legacy chip		0	1	
			New chip		1.12	2.25	
		$V_{ON/OFF}$ < 0.15 V, V_{IN} = 16 V, –40°C ≤ T_J ≤ 125°C	Legacy chip		0.01	2	
			New chip		1.12	2.75	
V_{UVLO+}	Rising bias supply UVLO	V_{IN} rising, –40°C ≤ T_J ≤ 125°C	New chip		2.2	2.4	V
V_{UVLO-}	Falling bias supply UVLO	V_{IN} falling, –40°C ≤ T_J ≤ 125°C		1.9			V
$V_{UVLO(HYST)}$	UVLO hysteresis	–40°C ≤ T_J ≤ 125°C			0.130		V
$V_{ON/\overline{OFF}}$	ON/$\overline{\text{OFF}}$ input voltage	Low = Output OFF	Legacy chip		0.55		V
			New chip		0.72		
		Low = Output OFF, V_{OUT} + 1 ≤ V_{IN} ≤ 16 V, –40°C ≤ T_J ≤ 125°C	Legacy chip			0.15	
			New chip			0.15	
		High = Output ON	Legacy chip		1.4		
			New chip		0.85		
		High = Output ON, V_{OUT} + 1 ≤ V_{IN} ≤ 16 V, –40°C ≤ T_J ≤ 125°C	Legacy chip	1.6			
			New chip	1.6			

6.5 Electrical Characteristics (continued)

specified at T_J = 25°C, V_{IN} = $V_{OUT(nom)}$ + 1.0 V or VIN = 2.5 V (whichever is greater), I_{OUT} = 1 mA, $V_{ON/OFF}$ = 2 V, C_{IN} = 1.0 μF, and C_{OUT} = 2.2 μF (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
$I_{ON/\overline{OFF}}$	ON/OFF input current	$V_{ON/OFF}$ = 0 V	Legacy chip		0.01		μA
			New chip		0.42		
		$V_{ON/OFF}$ = 0 V, V_{OUT} + 1 ≤ V_{IN} ≤ 16 V, –40°C ≤ T_J ≤ 125°C	Legacy chip			-1	
			New chip			-0.9	
		$V_{ON/OFF}$ = 5 V	Legacy chip		5		
			New chip		0.011		
		$V_{ON/OFF}$ = 5 V, V_{OUT} + 1 ≤ V_{IN} ≤ 16 V, –40°C ≤ T_J ≤ 125°C	Legacy chip			15	
			New chip			2.20	
IO(PK)	Peak output current	V_{OUT} ≥ $V_{O(NOM)}$ – 5% (steady state)	Legacy chip	300	350		mA
			New chip	300	350		
$I_{O(SC)}$	Short output current	R_L = 0 Ω (steady state)	Legacy chip		400		
			New chip		375		
$\Delta V_O / \Delta V_{IN}$	Ripple rejection	f = 1 kHz, C_{BYPASS} = 10 nF, C_{OUT} = 10 μF	Legacy chip		45		dB
			New chip		78		
V_n	Output noise voltage	Bandwidth = 300 Hz to 50 kHz, C_{BYPASS} = 10 nF, C_{OUT} = 2.2 μF, V_{OUT} = 3.3 V, I_{LOAD} = 150 mA	Legacy chip		30		μVRMS
		Bandwidth = 300 Hz to 50 kHz, C_{BYPASS} = 10 nF, C_{OUT} = 2.2 μF, V_{OUT} = 3.3 V, I_{LOAD} = 150 mA	New chip		30		
T_{sd+}	Thermal shutdown threshold	Shutdown, temperature increasing	New chip		170		°C
T_{sd-}		Reset, temperature decreasing			150		

(1) Dropout voltage (V_{DO}) is defined as the input-to-output differential at which the output voltage drops 100 mV below the value measured with a 1 V differential. V_{DO} is measured with V_{IN} = $V_{OUT(nom)}$ – 100 mV for fixed output devices.

6.6 Typical Characteristics

at operating temperature T_J = 25°C, V_{IN} = $V_{OUT(NOM)}$ + 1.0 V or 2.5 V (whichever is greater), I_{OUT} = 1 mA, ON/$\overline{OFF}$ pin tied to V_{IN}, C_{IN} = 1.0 μF, and C_{OUT} = 4.7 μF (unless otherwise noted)

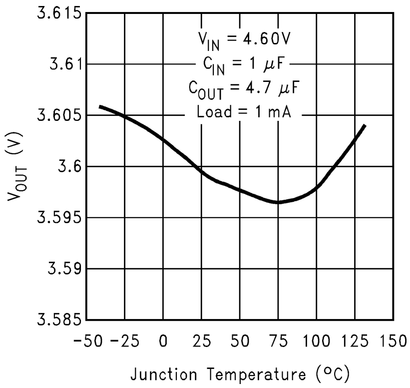


图 6-1. V_{OUT} vs Temperature for Legacy Chip

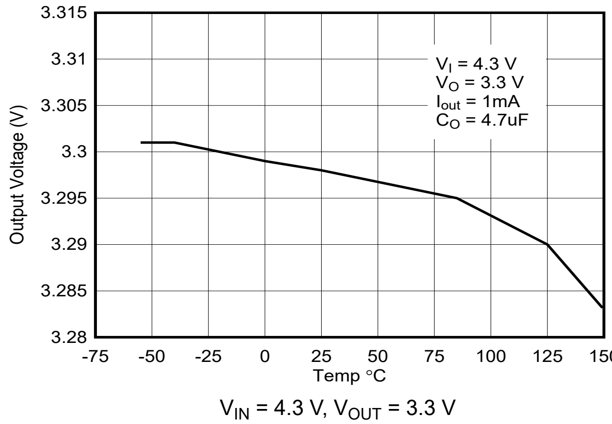


图 6-2. V_{OUT} vs Temperature for New Chip

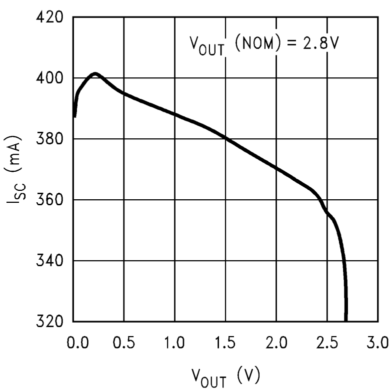


图 6-3. Short-Circuit Current vs Output Voltage for Legacy Chip

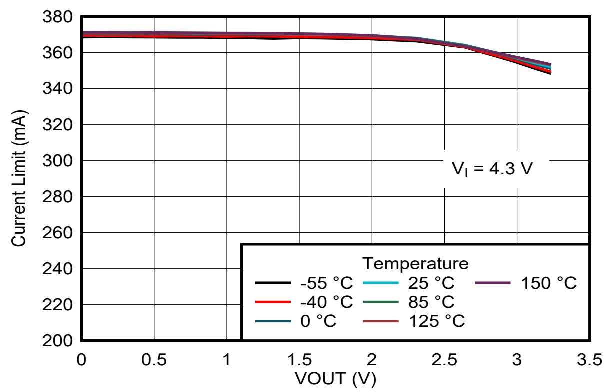


图 6-4. Short-Circuit Current vs Output Voltage for New Chip

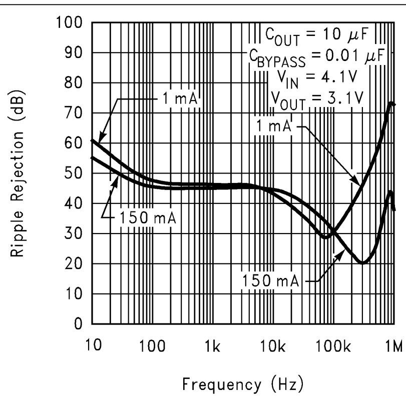


图 6-5. Ripple Rejection vs Frequency for Legacy Chip

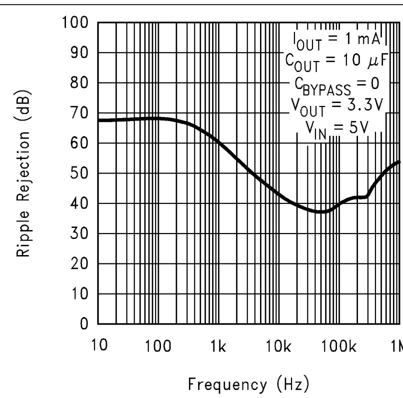


图 6-6. Ripple Rejection vs Frequency for Legacy Chip

6.6 Typical Characteristics (continued)

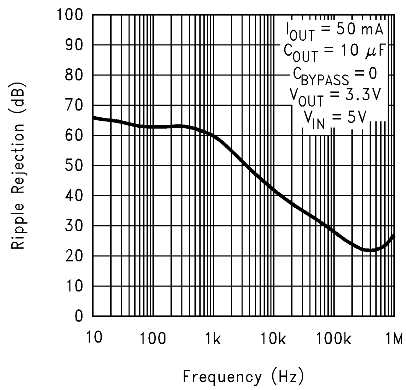


图 6-7. Ripple Rejection vs Frequency for Legacy Chip

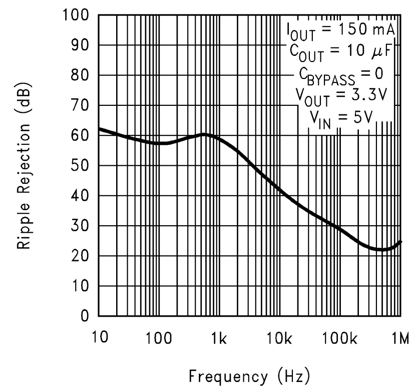
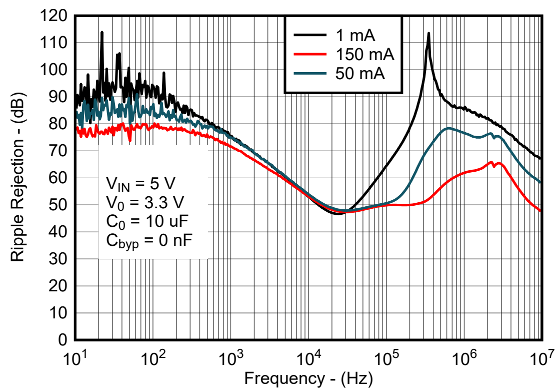


图 6-8. Ripple Rejection vs Frequency for Legacy Chip



V_{IN} = 5 V, V_{OUT} = 3.3 V, C_{OUT} = 10 μF, C_{BYP} = 0 nF

图 6-9. Ripple Rejection vs Frequency for New Chip

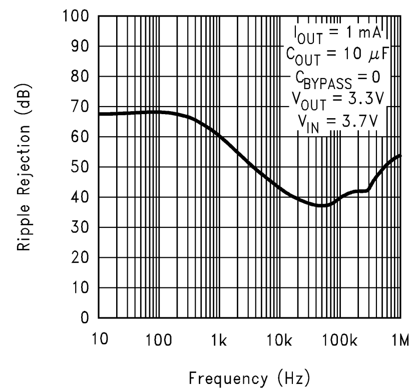


图 6-10. Ripple Rejection vs Frequency for Legacy Chip

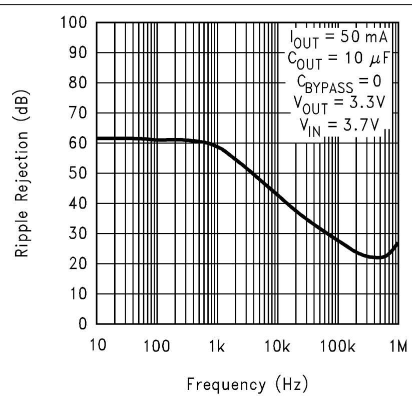


图 6-11. Ripple Rejection vs Frequency for Legacy Chip

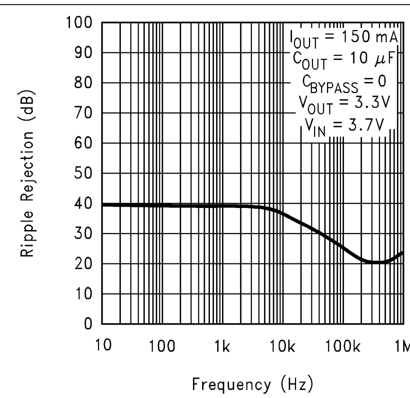


图 6-12. Ripple Rejection vs Frequency for Legacy Chip

6.6 Typical Characteristics (continued)

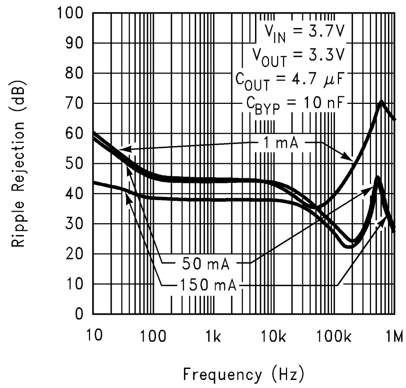
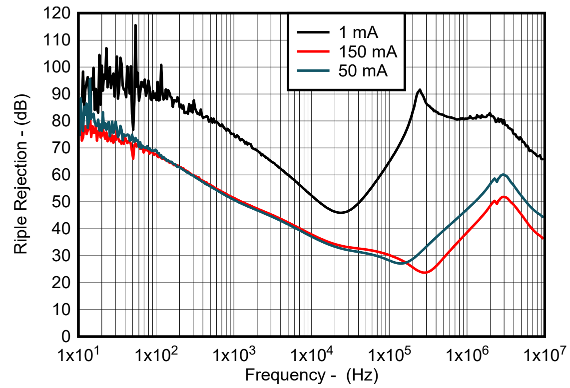


图 6-13. Ripple Rejection vs Frequency for Legacy Chip



V_{IN} = 3.7 V, V_{OUT} = 3.3 V, C_{OUT} = 10 μF, C_{BYP} = 0 nF

图 6-14. Ripple Rejection vs Frequency for New Chip

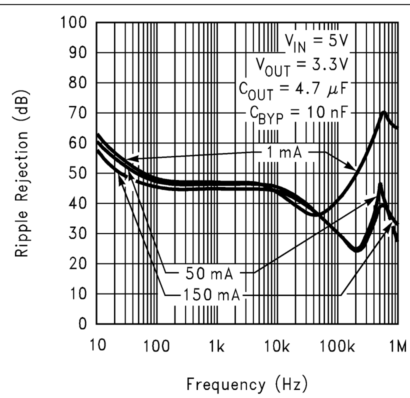


图 6-15. Ripple Rejection vs Frequency for Legacy Chip

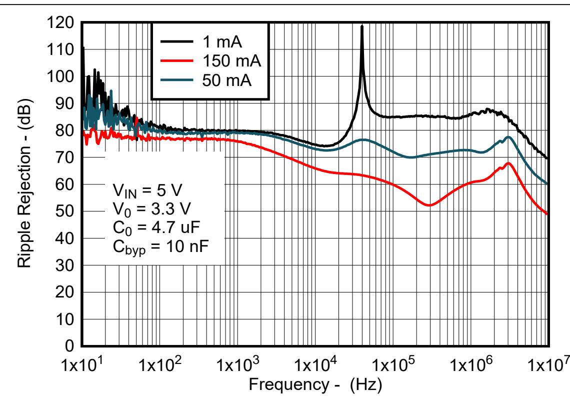


图 6-16. Ripple Rejection vs Frequency for New Chip

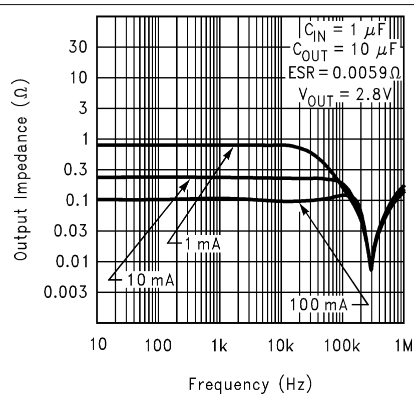


图 6-17. Output Impedance vs Frequency for Legacy Chip

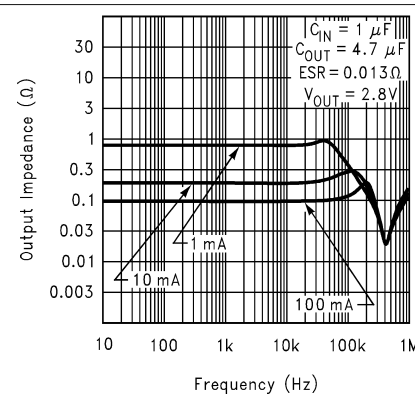


图 6-18. Output Impedance vs Frequency for Legacy Chip

6.6 Typical Characteristics (continued)

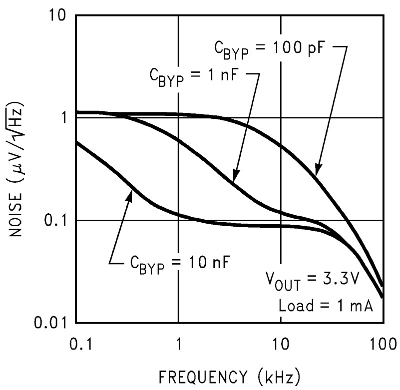


图 6-19. Output Noise Density for Legacy Chip

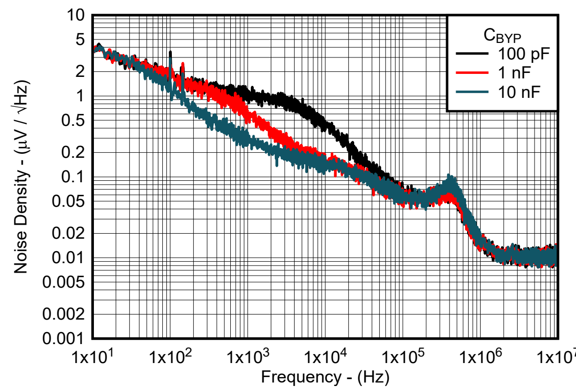


图 6-20. Output Noise Density vs Frequency for New Chip

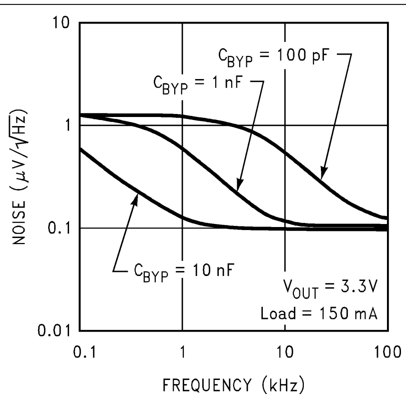


图 6-21. Output Noise Density for Legacy Chip

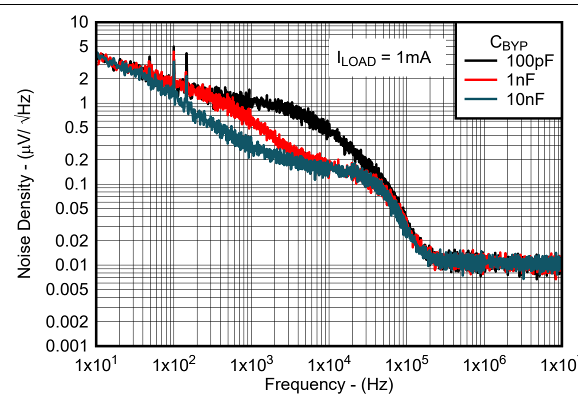


图 6-22. Output Noise Density vs Frequency for New Chip

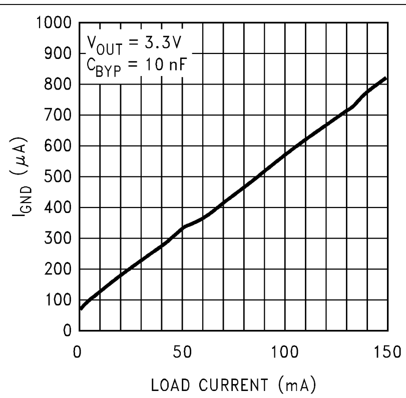


图 6-23. Ground Pin vs Load Current for Legacy Chip

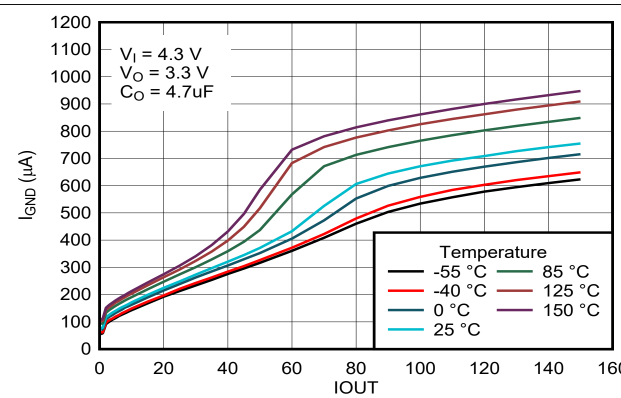


图 6-24. Ground Pin Current vs Load Current for New Chip

6.6 Typical Characteristics (continued)

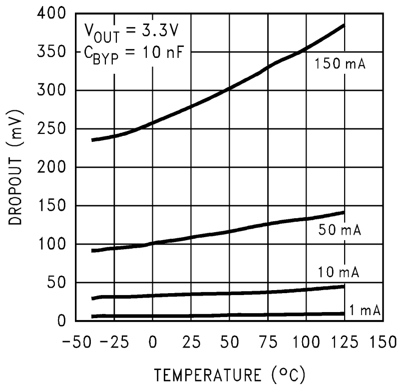


图 6-25. Dropout Voltage vs Temperature for Legacy Chip

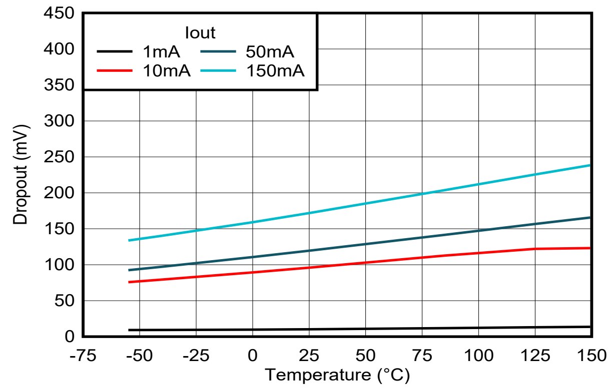


图 6-26. Dropout Voltage vs Temperature for New Chip

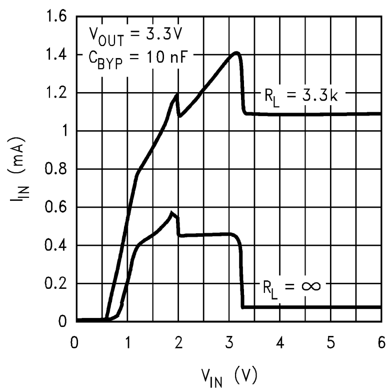


图 6-27. Input Current vs V_{IN} for Legacy Chip

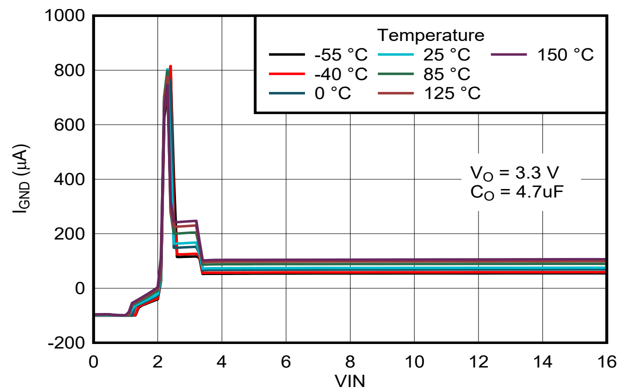


图 6-28. Input Current vs V_{IN} for New Chip

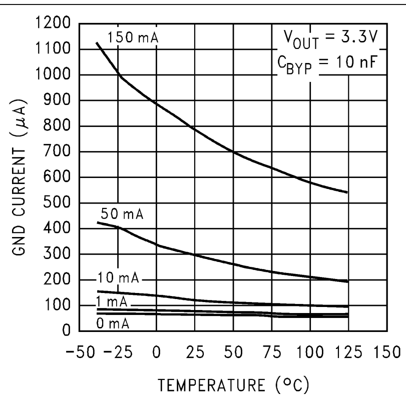


图 6-29. GND Pin Current vs Temperature for Legacy Chip

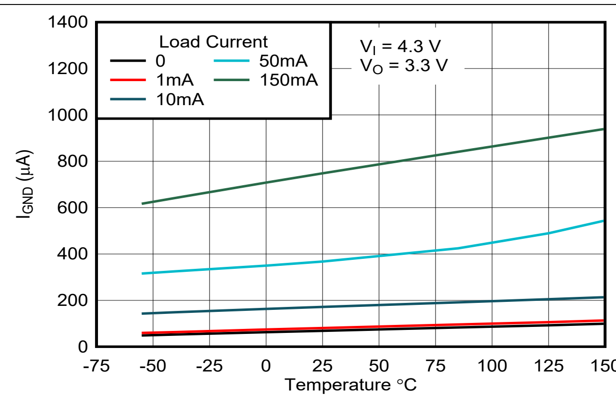


图 6-30. GND Pin Current vs Temperature for New Chip

6.6 Typical Characteristics (continued)

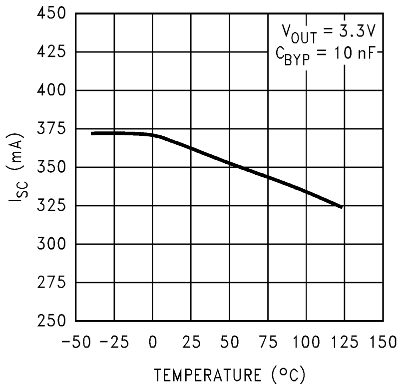


图 6-31. Instantaneous Short-Circuit Current for Legacy Chip

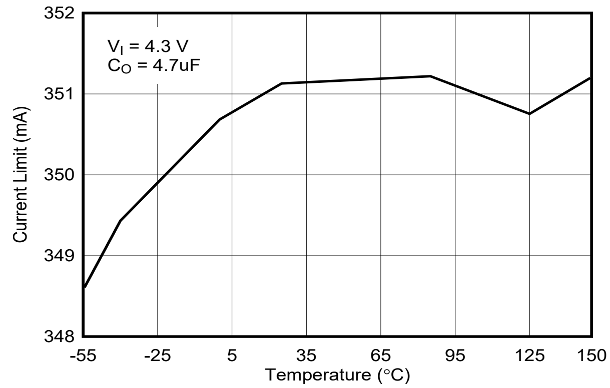


图 6-32. Short-Circuit Current vs Temperature for New Chip

7 Detailed Description

7.1 Overview

The LP2985-N is a fixed-output, low-noise, high PSRR, low-dropout regulator that offers exceptional, cost-effective performance for both portable and nonportable applications. The LP2985-N has an output tolerance of 1% across line, load, and temperature variation (for the new chip) and is capable of delivering 150 mA of continuous load current.

This device features integrated overcurrent protection, thermal shutdown, output enable, and internal output pulldown and has a built-in soft-start mechanism for controlled inrush current. This device delivers excellent line and load transient performance. The operating ambient temperature range of the device is from –40°C to +125°C.

7.2 Functional Block Diagrams

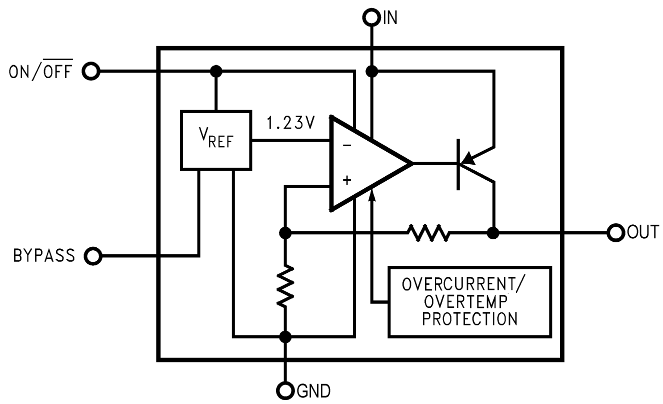


图 7-1. Block Diagram for Legacy Chip

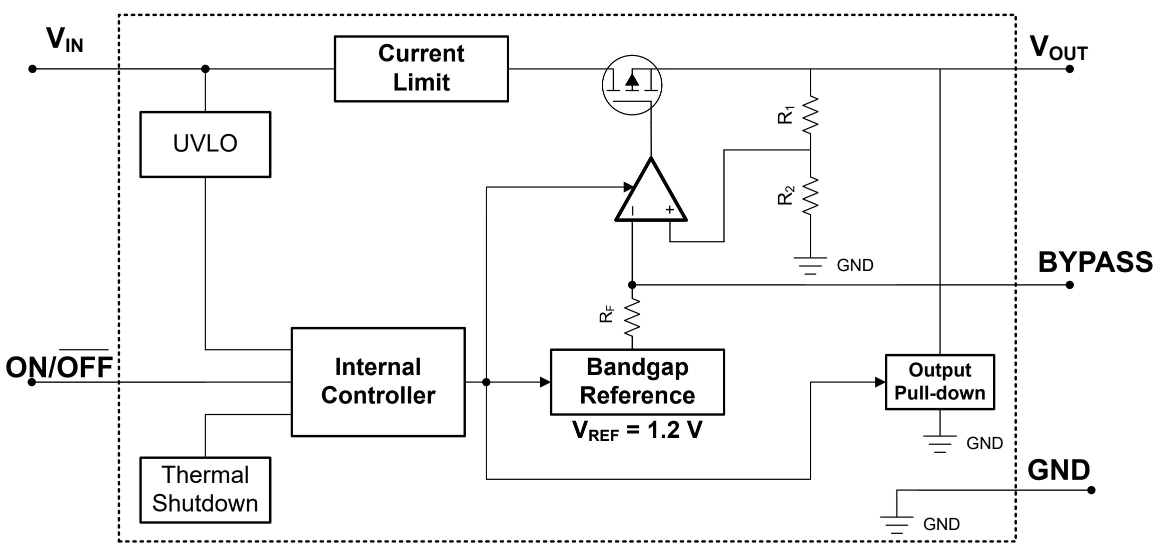


图 7-2. Block Diagram for New Chip

7.3 Feature Description

7.3.1 Output Enable

The ON/$\overline{\text{OFF}}$ pin for the device is an active-high pin. The output voltage is enabled when the voltage of the ON/$\overline{\text{OFF}}$ pin is greater than the high-level input voltage of the ON/$\overline{\text{OFF}}$ pin and disabled with the ON/$\overline{\text{OFF}}$ pin voltage is less than the low-level input voltage of the ON/$\overline{\text{OFF}}$ pin. If independent control of the output voltage is not needed, connect the ON/$\overline{\text{OFF}}$ pin to the input of the device.

The device has an internal pulldown circuit that activates when the device is disabled by pulling the ON/$\overline{\text{OFF}}$ pin voltage lower than the low-level input voltage of the ON/$\overline{\text{OFF}}$ pin to actively discharge the output voltage.

7.3.2 Dropout Voltage

Dropout voltage (V_{DO}) is defined as the input voltage minus the output voltage (V_{IN} – V_{OUT}) at the rated output current (I_{RATED}), where the pass transistor is fully on. I_{RATED} is the maximum I_{OUT} listed in the *Recommended Operating Conditions* table. The pass transistor is in the ohmic or triode region of operation, and acts as a switch. The dropout voltage indirectly specifies a minimum input voltage greater than the nominal programmed output voltage at which the output voltage is expected to stay in regulation. If the input voltage falls to less than the nominal output regulation, then the output voltage falls as well.

For a CMOS regulator, the dropout voltage is determined by the drain-source on-state resistance ($R_{DS(ON)}$) of the pass transistor. Therefore, if the linear regulator operates at less than the rated current, the dropout voltage for that current scales accordingly. The following equation calculates the $R_{DS(ON)}$ of the device.

$$R_{DS(ON)} = \frac{V_{DO}}{I_{RATED}} \tag{1}$$

7.3.3 Current Limit

The device has an internal current limit circuit that protects the regulator during transient high-load current faults or shorting events. The current limit is a brick-wall scheme. In a high-load current fault, the brick-wall scheme limits the output current to the current limit (I_{CL}). I_{CL} is listed in the *Electrical Characteristics* table.

The output voltage is not regulated when the device is in current limit. When a current limit event occurs, the device begins to heat up because of the increase in power dissipation. When the device is in brick-wall current limit, the pass transistor dissipates power [(V_{IN} – V_{OUT}) × I_{CL}]. If thermal shutdown is triggered, the device turns off. After the device cools down, the internal thermal shutdown circuit turns the device back on. If the output current fault condition continues, the device cycles between current limit and thermal shutdown. For more information on current limits, see the *Know Your Limits* application note.

图 7-3 shows a diagram of the current limit.

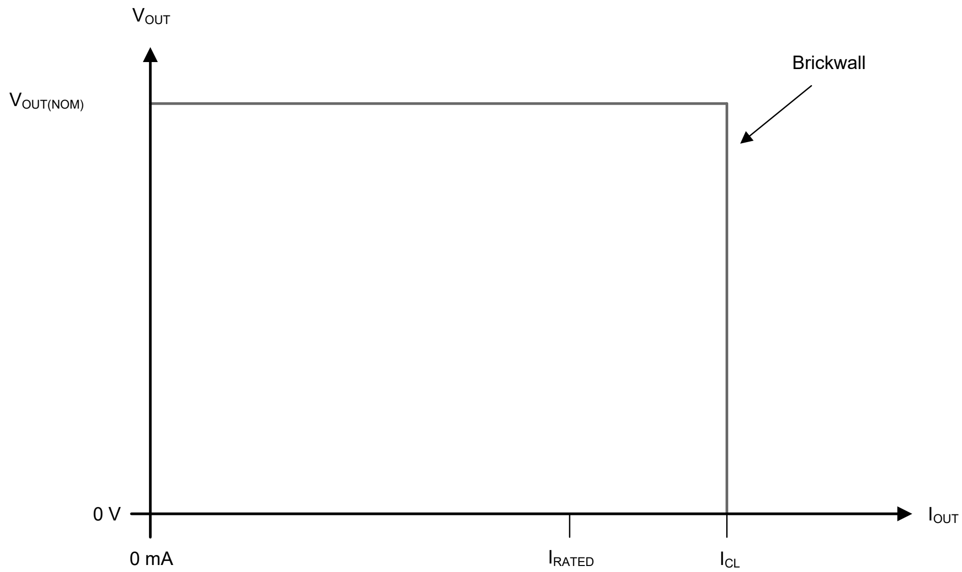


图 7-3. Current Limit

7.3.4 Undervoltage Lockout (UVLO)

The device has an independent undervoltage lockout (UVLO) circuit that monitors the input voltage, allowing a controlled and consistent turn on and off of the output voltage. To prevent the device from turning off if the input drops during turn on, the UVLO has hysteresis as specified in the *Electrical Characteristics* table.

7.3.5 Output Pulldown

The new chip has an output pulldown circuit. The output pulldown activates in the following conditions:

- When the device is disabled ($V_{ON/\overline{OFF}} < V_{ON/\overline{OFF}(LOW)}$)
- If 1.0 V < V_{IN} < V_{UVLO}

Do not rely on the output pulldown circuit for discharging a large amount of output capacitance after the input supply has collapsed because reverse current can flow from the output to the input. This reverse current flow can cause damage to the device. See the *Reverse Current* section for more details.

7.3.6 Thermal Shutdown

The device contains a thermal shutdown protection circuit to disable the device when the junction temperature (T_J) of the pass transistor rises to $T_{SD(shutdown)}$ (typical). Thermal shutdown hysteresis assures that the device resets (turns on) when the temperature falls to $T_{SD(reset)}$ (typical).

The thermal time-constant of the semiconductor die is fairly short, thus the device can cycle on and off when thermal shutdown is reached until power dissipation is reduced. Power dissipation during start up can be high from large V_{IN} – V_{OUT} voltage drops across the device or from high inrush currents charging large output capacitors. Under some conditions, the thermal shutdown protection disables the device before start up completes.

For reliable operation, limit the junction temperature to the maximum listed in the *Recommended Operating Conditions* table. Operation above this maximum temperature causes the device to exceed operational specifications. Although the internal protection circuitry of the device is designed to protect against thermal overall conditions, this circuitry is not intended to replace proper heat sinking. Continuously running the device into thermal shutdown or above the maximum recommended junction temperature reduces long-term reliability.

7.4 Device Functional Modes

7.4.1 Device Functional Mode Comparison

表 7-1 shows the conditions that lead to the different modes of operation. See the *Electrical Characteristics* table for parameter values.

表 7-1. Device Functional Mode Comparison

OPERATING MODE	PARAMETER			
	V_{IN}	$V_{ON/\overline{OFF}}$	I_{OUT}	T_J
Normal operation	$V_{IN} > V_{OUT(nom)} + V_{DO}$ and $V_{IN} > V_{IN(min)}$	$V_{ON/\overline{OFF}} > V_{ON/\overline{OFF}(HI)}$	$I_{OUT} < I_{OUT(max)}$	$T_J < T_{SD(shutdown)}$
Dropout operation	$V_{IN(min)} < V_{IN} < V_{OUT(nom)} + V_{DO}$	$V_{ON/\overline{OFF}} > V_{ON/\overline{OFF}(HI)}$	$I_{OUT} < I_{OUT(max)}$	$T_J < T_{SD(shutdown)}$
Disabled (any true condition disables the device)	$V_{IN} < V_{UVLO}$	$V_{ON/\overline{OFF}} < V_{ON/\overline{OFF}(LOW)}$	Not applicable	$T_J > T_{SD(shutdown)}$

7.4.2 Normal Operation

The device regulates to the nominal output voltage when the following conditions are met:

- The input voltage is greater than the nominal output voltage plus the dropout voltage ($V_{OUT(nom)} + V_{DO}$)
- The output current is less than the current limit ($I_{OUT} < I_{CL}$)
- The device junction temperature is less than the thermal shutdown temperature ($T_J < T_{SD}$)
- The ON/$\overline{\text{OFF}}$ voltage has previously exceeded the ON/$\overline{\text{OFF}}$ rising threshold voltage and has not yet decreased to less than the enable falling threshold

7.4.3 Dropout Operation

If the input voltage is lower than the nominal output voltage plus the specified dropout voltage, but all other conditions are met for normal operation, the device operates in dropout mode. In this mode, the output voltage tracks the input voltage. During this mode, the transient performance of the device becomes significantly degraded because the pass transistor is in the ohmic or triode region, and acts as a switch. Line or load transients in dropout can result in large output voltage deviations.

When the device is in a steady dropout state (defined as when the device is in dropout, $V_{IN} < V_{OUT(NOM)} + V_{DO}$, directly after being in a normal regulation state, but *not* during start up), the pass transistor is driven into the ohmic or triode region. When the input voltage returns to a value greater than or equal to the nominal output voltage plus the dropout voltage ($V_{OUT(NOM)} + V_{DO}$), the output voltage can overshoot for a short period of time while the device pulls the pass transistor back into the linear region.

7.4.4 Disabled

The output of the device can be shutdown by forcing the voltage of the ON/$\overline{\text{OFF}}$ pin to less than the maximum ON/$\overline{\text{OFF}}$ pin low-level input voltage (see the *Electrical Characteristics* table). When disabled, the pass transistor is turned off, internal circuits are shutdown, and the output voltage is actively discharged to ground by an internal discharge circuit from the output to ground.

8 Application and Implementation

备注

以下应用部分中的信息不属于 TI 器件规格的范围，TI 不担保其准确性和完整性。TI 的客 户应负责确定器件是否适用于其应用。客户应验证并测试其设计，以确保系统功能。

8.1 Application Information

The LP2985-N is a linear voltage regulator operating from 2.5 V to 16 V on the input and regulates voltages between 1.2 V to 5 V (for the new chip) with 1% accuracy across line, load and temperature (for the new chip) and 150-mA maximum output current. The LP2985-N low output noise of 30 μV_{RMS} (with 10-nF bypass capacitors) and wide bandwidth PSRR performance of greater than 70 dB at 1 kHz and 40 dB at 1 MHz help attenuate the switching frequency of an upstream DC/DC converter and minimize post regulator filtering.

8.1.1 Recommended Capacitor Types

The device is designed to be stable using low equivalent series resistance (ESR) ceramic capacitors at the input and output. Multilayer ceramic capacitors have become the industry standard for these types of applications and are recommended, but must be used with good judgment. Ceramic capacitors that employ X7R-, X5R-, and C0G-rated dielectric materials provide relatively good capacitive stability across temperature, whereas the use of Y5V-rated capacitors is discouraged because of large variations in capacitance.

Regardless of the ceramic capacitor type selected, the effective capacitance varies with operating voltage and temperature. Generally, expect the effective capacitance to decrease by as much as 50%. The input and output capacitors listed in the *Recommended Operating Conditions* table account for an effective capacitance of approximately 50% of the nominal value.

8.1.2 Input and Output Capacitor Requirements

Although an input capacitor is not required for stability, good analog design practice is to connect a capacitor from IN to GND. This capacitor counteracts reactive input sources and improves transient response, input ripple, and PSRR. Use an input capacitor if the source impedance is more than 0.5 Ω. A higher value capacitor can be necessary if large, fast rise-time load or line transients are anticipated or if the device is located several inches from the input power source.

Dynamic performance of the device is improved with the use of an output capacitor. Use an output capacitor within the range specified in the *Recommended Operating Conditions* table for stability.

8.1.3 Noise Bypass Capacitor (C_{BYPASS})

The LP2985-N allows for low-noise performance with the use of a bypass capacitor that is connected to the internal band-gap reference with the BYPASS pin. This high-impedance band-gap circuitry is biased in the microampere range and, thus, cannot be loaded significantly, otherwise, the output (and, correspondingly, the output of the regulator) changes. Thus, for best output accuracy, dc leakage current through C_{BYPASS} must be minimized as much as possible and must never exceed 100 nA. The C_{BYPASS} capacitor also impacts the start-up behavior of the regulator. Inrush current and start-up time increase with larger bypass capacitor values.

Use a 10-nF capacitor for C_{BYPASS}. Ceramic and film capacitors are good choices for this purpose.

8.1.4 Reverse Current

Excessive reverse current can damage this device. Reverse current flows through the intrinsic body diode of the pass transistor instead of the normal conducting channel. At high magnitudes, this current flow degrades the long-term reliability of the device.

Conditions where reverse current can occur are outlined in this section, all of which can exceed the absolute maximum rating of $V_{OUT} \leqslant V_{IN}$ + 0.3 V.

- If the device has a large C_{OUT} and the input supply collapses with little or no load current
- The output is biased when the input supply is not established
- The output is biased above the input supply

If reverse current flow is expected in the application, use external protection to protect the device. Reverse current is not limited in the device, so external limiting is required if extended reverse voltage operation is anticipated.

图 8-1 shows one approach for protecting the device.

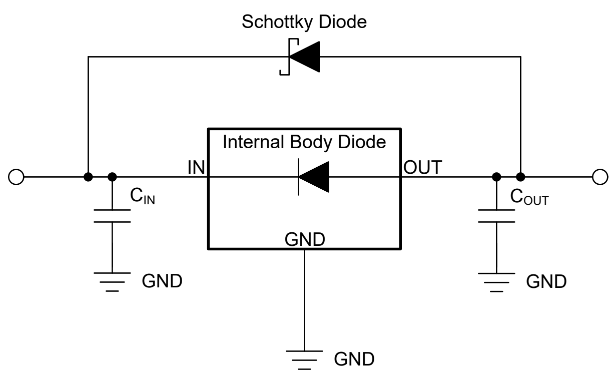


图 8-1. Example Circuit for Reverse Current Protection Using a Schottky Diode

8.1.5 Power Dissipation (P_D)

Circuit reliability requires consideration of the device power dissipation, location of the circuit on the printed circuit board (PCB), and correct sizing of the thermal plane. The PCB area around the regulator must have few or no other heat-generating devices that cause added thermal stress.

To first-order approximation, power dissipation in the regulator depends on the input-to-output voltage difference and load conditions. The following equation calculates power dissipation (P_D).

$$P_D = (V_{IN} - V_{OUT}) \times I_{OUT} \quad (2)$$

备注

Power dissipation can be minimized, and therefore greater efficiency can be achieved, by correct selection of the system voltage rails. For the lowest power dissipation use the minimum input voltage required for correct output regulation.

For devices with a thermal pad, the primary heat conduction path for the device package is through the thermal pad to the PCB. Solder the thermal pad to a copper pad area under the device. This pad area must contain an array of plated vias that conduct heat to additional copper planes for increased heat dissipation.

The maximum power dissipation determines the maximum allowable ambient temperature (T_A) for the device. According to the following equation, power dissipation and junction temperature are most often related by the junction-to-ambient thermal resistance ($R_{\theta JA}$) of the combined PCB and device package and the temperature of the ambient air (T_A).

$$T_J = T_A + (R_{\theta JA} \times P_D) \tag{3}$$

Thermal resistance ($R_{\theta JA}$) is highly dependent on the heat-spreading capability built into the particular PCB design, and therefore varies according to the total copper area, copper weight, and location of the planes. The junction-to-ambient thermal resistance listed in the *Thermal Information* table is determined by the JEDEC standard PCB and copper-spreading area, and is used as a relative measure of package thermal performance.

8.1.6 Estimating Junction Temperature

The JEDEC standard now recommends the use of psi (Ψ) thermal metrics to estimate the junction temperatures of the linear regulator when in-circuit on a typical PCB board application. These metrics are not thermal resistance parameters and instead offer a practical and relative way to estimate junction temperature. These psi metrics are determined to be significantly independent of the copper area available for heat-spreading. The *Thermal Information* table lists the primary thermal metrics, which are the junction-to-top characterization parameter (ψ_{JT}) and junction-to-board characterization parameter (ψ_{JB}). These parameters provide two methods for calculating the junction temperature (T_J), as described in the following equations. Use the junction-to-top characterization parameter (ψ_{JT}) with the temperature at the center-top of device package (T_T) to calculate the junction temperature. Use the junction-to-board characterization parameter (ψ_{JB}) with the PCB surface temperature 1 mm from the device package (T_B) to calculate the junction temperature.

$$T_J = T_T + \psi_{JT} \times P_D \tag{4}$$

where:

- P_D is the dissipated power
- T_T is the temperature at the center-top of the device package

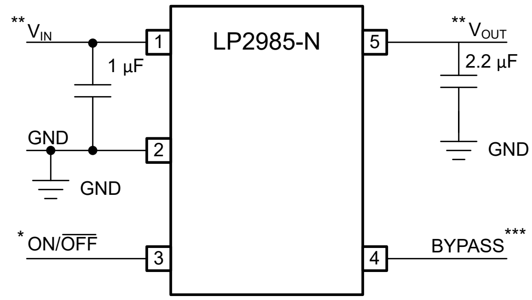
$$T_J = T_B + \psi_{JB} \times P_D \tag{5}$$

where:

- T_B is the PCB surface temperature measured 1 mm from the device package and centered on the package edge

For detailed information on the thermal metrics and how to use them, see the *Semiconductor and IC Package Thermal Metrics* application note.

8.2 Typical Application



*The ON/OFF input must be actively terminated. Tie to V_{IN} if this function is not used. **Minimum capacitance is shown to ensure stability (can be increased without limit). Ceramic capacitor required for output (see the *Input and Output Capacitor Requirements* section). ***Reduces output noise (can be omitted if application is not noise critical). Use ceramic or film type with very low leakage current (see the *Noise Bypass Capacitor (C_{BYPASS})* section).

图 8-2. Typical Application Schematic

8.2.1 Design Requirements

表 8-1 lists the typical design parameters.

表 8-1. Design Parameters for the New Chip

DESIGN PARAMETERS	VALUE
Input voltage	4.3 V, ±10% provided by the DC/DC converter switching at 1 MHz
Output voltage	3.3 V, ±1%
Output current	0 mA – 150 mA (maximum)
RMS noise, 300 Hz to 50 kHz	< 30 μV_{RMS}
PSRR at 100 kHz	> 40 dB

8.2.2 Detailed Design Procedure

8.2.2.1 Capacitor Characteristics

The LP2985-N was designed to work with ceramic capacitors on the output to take advantage of the benefits these capacitors offer. For capacitance values in the 2.2-μF to 4.7-μF range, ceramics are the least expensive and also have the lowest ESR values (which makes these components the most efficient at eliminating high-frequency noise). The ESR of a typical 2.2-μF ceramic capacitor is in the range of 10 mΩ to 20 mΩ, which easily meets the ESR limits required for stability by the LP2985-N.

One disadvantage of ceramic capacitors is that the capacitance can vary with temperature. Most large-value ceramic capacitors (⩾ 2.2 μF) are manufactured with the Z5U or Y5V temperature characteristic, which results in the capacitance dropping by more than 50% as the temperature goes from 25°C to 85°C.

This capacitance drop can cause problems if a 2.2-μF capacitor is used on the output because that capacitor can down to approximately 1 μF at high ambient temperatures (which can cause the LM2985 to oscillate). If Z5U or Y5V capacitors are used on the output, a minimum capacitance value of 2.2 μF must be observed.

A better choice for temperature coefficient in ceramic capacitors is X7R, which holds the capacitance within ±15%. Unfortunately, the larger values of capacitance are not offered by all manufacturers in the X7R dielectric.

Tantalum capacitors are less desirable than ceramics for use as output capacitors because they are more expensive when comparing equivalent capacitance and voltage ratings in the 1-μF to 4.7-μF range.

Another important consideration is that tantalum capacitors have higher ESR values than equivalent size ceramics. Which means that although a tantalum capacitor can possibly have an ESR value within the stable range, the capacitor must be larger in capacitance (which means bigger and more costly) than a ceramic capacitor with the same ESR value.

The ESR of a typical tantalum increases by approximately 2:1 as the temperature goes from 25°C down to –40°C, so some guard band must be allowed.

8.2.2.2 ON/$\overline{\text{OFF}}$ Input Operation

The LP2985-N is shut off by driving the ON/$\overline{\text{OFF}}$ input low, and turned on by pulling the ON/$\overline{\text{OFF}}$ input high. If this feature is not used, the ON/$\overline{\text{OFF}}$ input must be tied to V_{IN} to keep the regulator output on at all times.

To provide proper operation, the signal source used to drive the ON/$\overline{\text{OFF}}$ input must be able to swing above and below the specified turn-on/turn-off voltage thresholds listed in the *Electrical Characteristics* section under $V_{ON/\overline{OFF}}$. For the legacy chip, to prevent misoperation, the turn-on (and turn-off) voltage signals applied to the ON/$\overline{\text{OFF}}$ input must have a slew rate that is ⩾ 40 mV/µs. But for the new chip, there is no restriction on the slew rate of the voltage signals applied to the ON/$\overline{\text{OFF}}$ pin.

8.2.3 Application Curves

at operating temperature T_J = 25°C, V_{IN} = $V_{OUT(NOM)}$ + 1.0 V or 2.5 V (whichever is greater), I_{OUT} = 1 mA, ON/$\overline{\text{OFF}}$ pin tied to V_{IN}, C_{IN} = 1.0 µF, and C_{OUT} = 4.7 µF (unless otherwise noted)

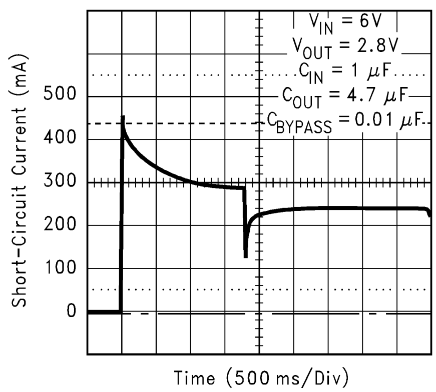


图 8-3. Short-Circuit Current for Legacy Chip at V_{IN} = 6 V

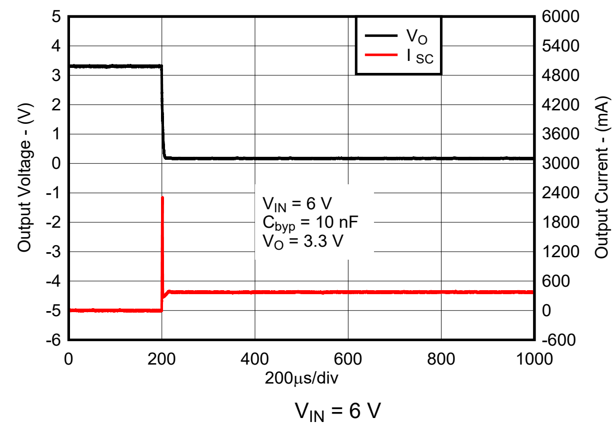


图 8-4. Short-Circuit Current for New Chip at V_{IN} = 6 V

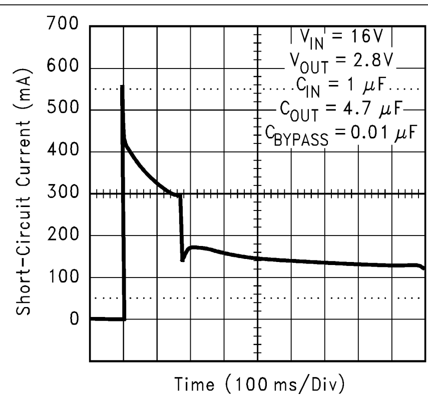


图 8-5. Short-Circuit Current for Legacy Chip at V_{IN} = 16 V

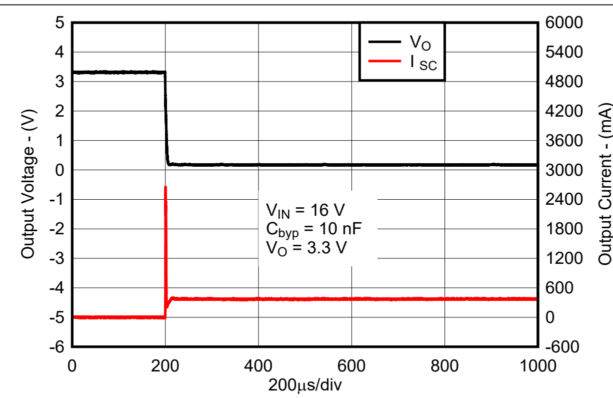


图 8-6. Short-Circuit Current for New Chip at V_{IN} = 16 V

8.2.3 Application Curves (continued)

at operating temperature T_J = 25°C, V_{IN} = $V_{OUT(NOM)}$ + 1.0 V or 2.5 V (whichever is greater), I_{OUT} = 1 mA, ON/$\overline{OFF}$ pin tied to V_{IN}, C_{IN} = 1.0 µF, and C_{OUT} = 4.7 µF (unless otherwise noted)

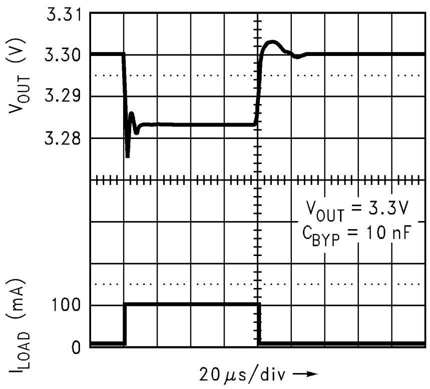
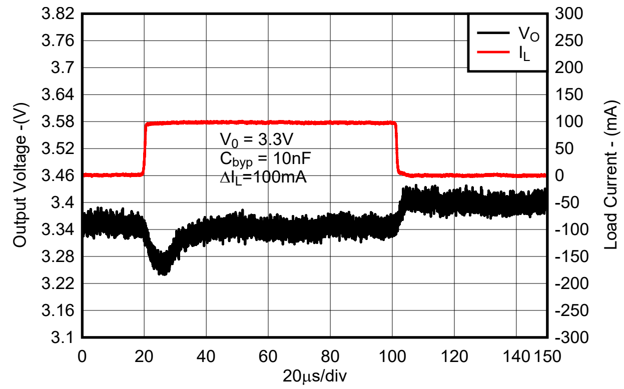


图 8-7. Load Transient Response for Legacy Chip



dI/dt = 1 A/ µ F

图 8-8. Load Transient Response for New Chip

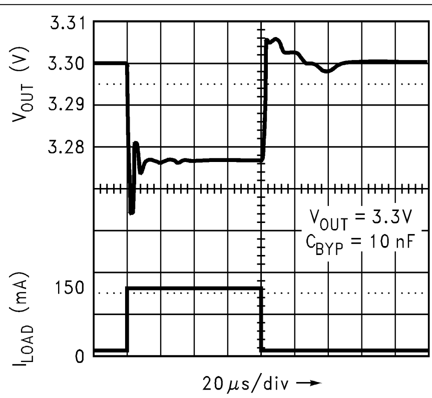
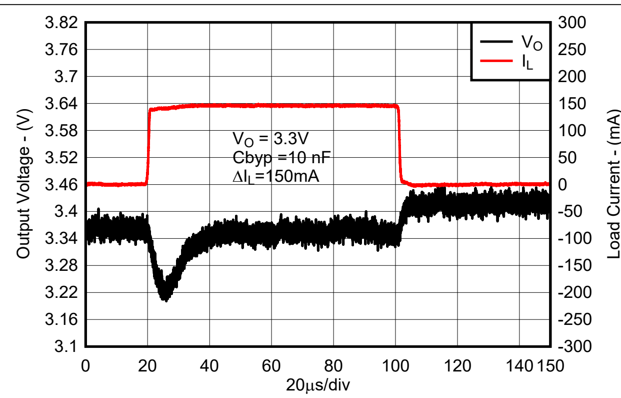


图 8-9. Load Transient Response for Legacy Chip



dI/dt = 1 A/ µ F

图 8-10. Load Transient for New Chip

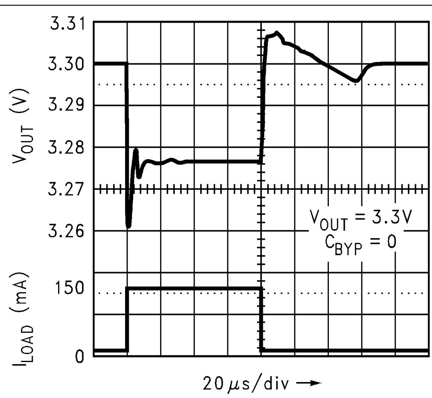
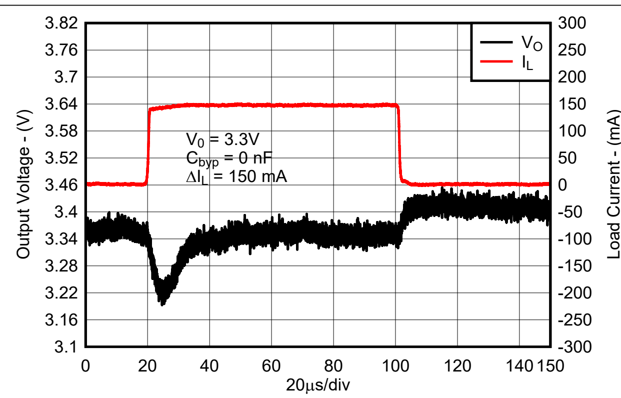


图 8-11. Load Transient Response for Legacy Chip



dI/dt = 1 A/ µ F

图 8-12. Load Transient Response for New Chip

8.2.3 Application Curves (continued)

at operating temperature T_J = 25°C, V_{IN} = $V_{OUT(NOM)}$ + 1.0 V or 2.5 V (whichever is greater), I_{OUT} = 1 mA, ON/$\overline{OFF}$ pin tied to V_{IN}, C_{IN} = 1.0 µF, and C_{OUT} = 4.7 µF (unless otherwise noted)

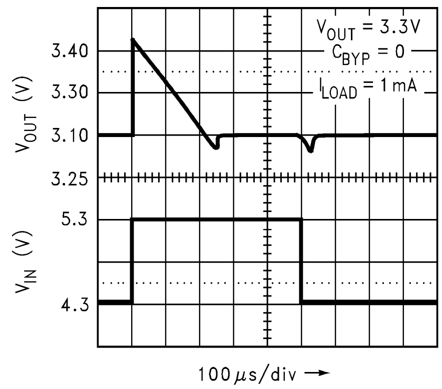
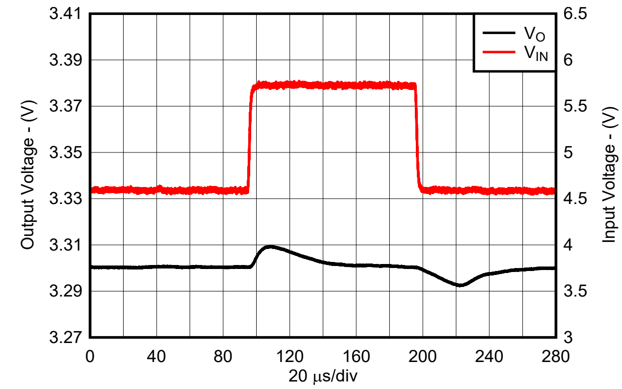


图 8-13. Line Transient Response for Legacy Chip



V_{OUT} = 3.3 V, C_{BYP} = 0 nF, ΔV_{IN} = 1 V, I_{OUT} = 1 mA, dV/dt = 1 V/ µ F

图 8-14. Line Transient Response for New Chip

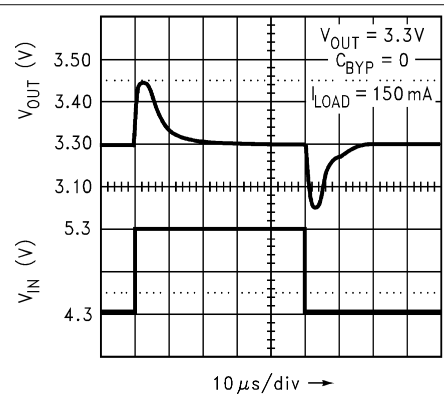
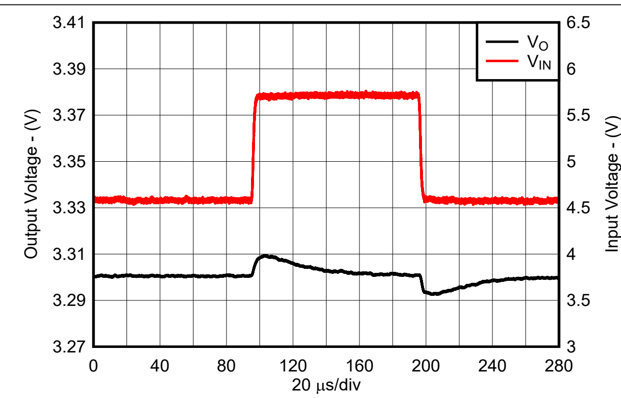


图 8-15. Line Transient Response for Legacy Chip



V_{OUT} = 3.3 V, C_{BYP} = 0 nF, ΔV_{IN} = 1 V, I_{OUT} = 150 mA, dV/dt = 1 V/ µ F

图 8-16. Line Transient Response for New Chip

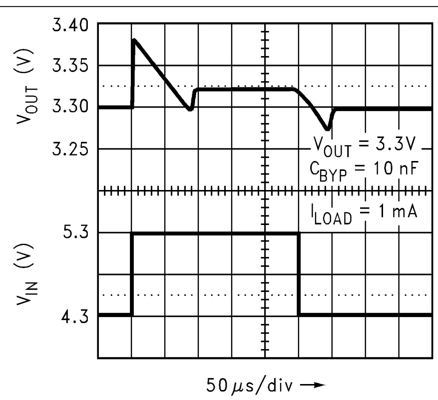
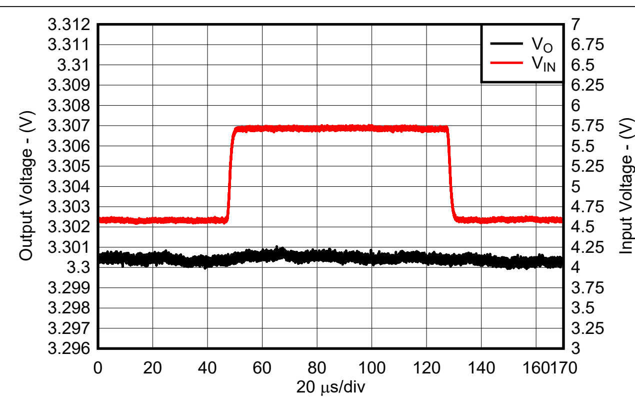


图 8-17. Line Transient Response for Legacy Chip



V_{OUT} = 3.3 V, C_{BYP} = 10 nF, ΔV_{IN} = 1 V, I_{OUT} = 1 mA, dV/dt = 1 V/ µ F

图 8-18. Line Transient Response for New Chip

8.2.3 Application Curves (continued)

at operating temperature T_J = 25°C, V_{IN} = $V_{OUT(NOM)}$ + 1.0 V or 2.5 V (whichever is greater), I_{OUT} = 1 mA, ON/$\overline{OFF}$ pin tied to V_{IN}, C_{IN} = 1.0 µF, and C_{OUT} = 4.7 µF (unless otherwise noted)

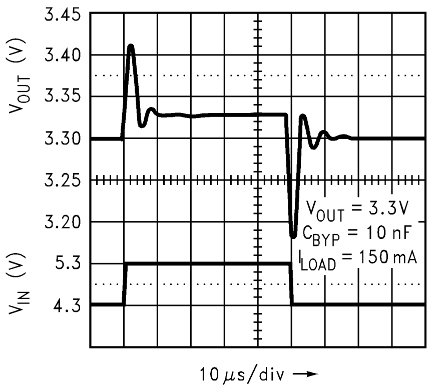
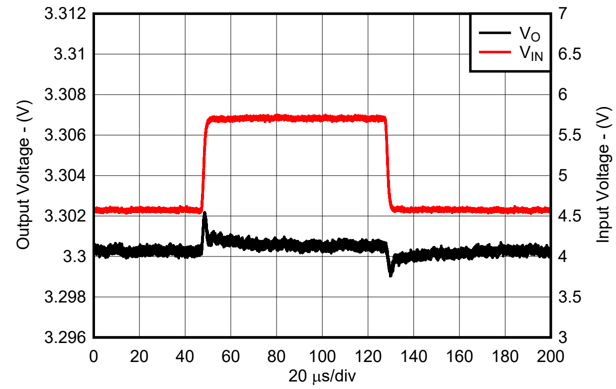


图 8-19. Line Transient Response for Legacy Chip



V_{OUT} = 3.3 V, C_{BYP} = 10 nF, ΔV_{IN} = 1 V, I_{OUT} = 150 mA, dV/dt = 1 V/µF

图 8-20. Line Transient Response for New Chip

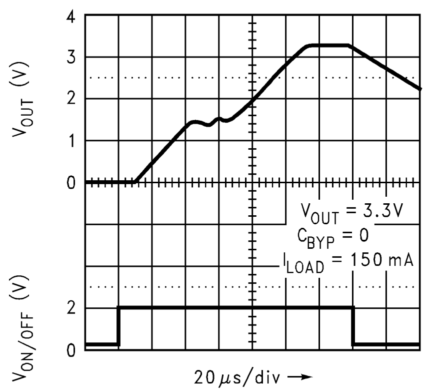


图 8-21. Turn-On Time for Legacy Chip

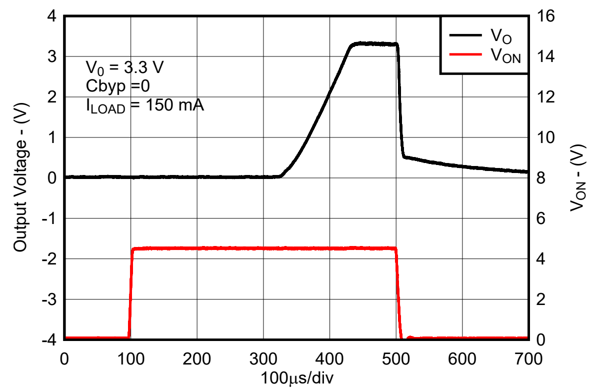


图 8-22. Turn-On Time for New Chip

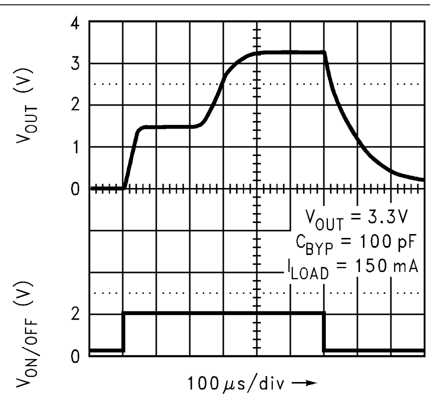


图 8-23. Turn-On Time for Legacy Chip

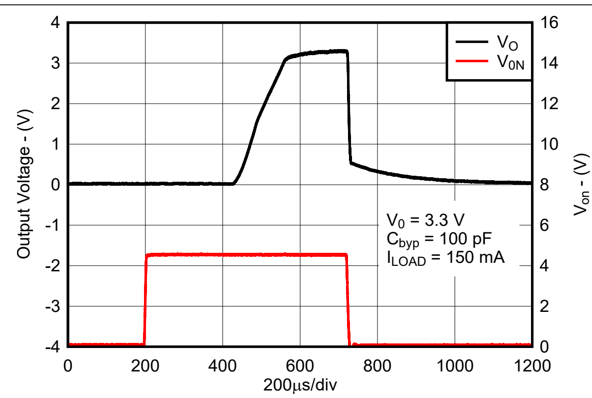


图 8-24. Turn-On Time for New Chip

8.2.3 Application Curves (continued)

at operating temperature T_J = 25°C, V_{IN} = $V_{OUT(NOM)}$ + 1.0 V or 2.5 V (whichever is greater), I_{OUT} = 1 mA, ON/$\overline{\text{OFF}}$ pin tied to V_{IN}, C_{IN} = 1.0 µF, and C_{OUT} = 4.7 µF (unless otherwise noted)

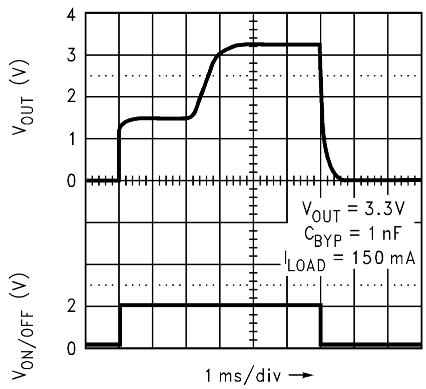


图 8-25. Turn-On Time for Legacy Chip

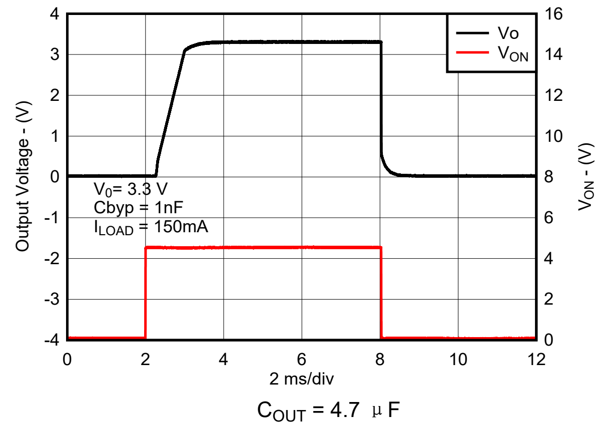


图 8-26. Turn-On Time for New Chip

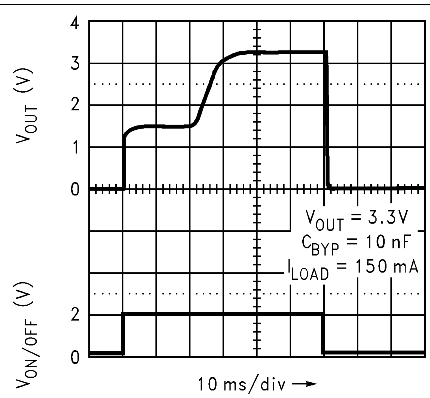


图 8-27. Turn-On Time for Legacy Chip

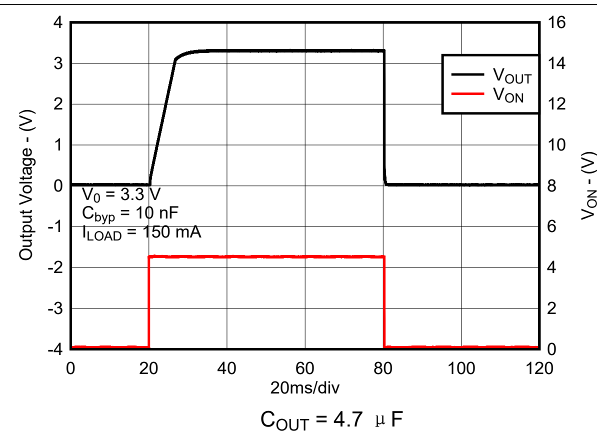


图 8-28. Turn-On Time for New Chip

8.3 Power Supply Recommendations

A power supply can be used at the input voltage within the ranges given in the *Recommended Operating Conditions* table. Use bypass capacitors as described in the *Layout Guidelines* section.

8.4 Layout

8.4.1 Layout Guidelines

For best overall performance, place all circuit components on the same side of the circuit board and as near as practical to the respective LDO pin connections. Place ground return connections to the input and output capacitor, and to the LDO ground pin as close as possible to each other, connected by a wide, component-side, copper surface. The use of vias and long traces to create LDO circuit connections is strongly discouraged and negatively affects system performance. This grounding and layout scheme minimizes inductive parasitics, and thereby reduces load-current transients, minimizes noise, and increases circuit stability.

A ground reference plane is also recommended and is either embedded in the PCB or located on the bottom side of the PCB opposite the components. This reference plane serves to assure accuracy of the output voltage, shield noise, and behaves similar to a thermal plane to spread (or sink) heat from the LDO device. In most applications, this ground plane is necessary to meet thermal requirements.

8.4.2 Layout Example

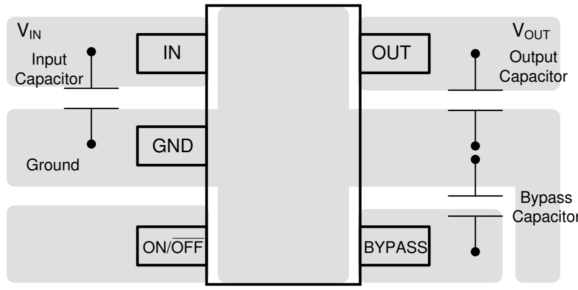


图 8-29. LP2985 SOT-23 Package Typical Layout

9 Device and Documentation Support

9.1 Documentation Support

9.1.1 Related Documentation

- Texas Instruments, *Semiconductor and IC Package Thermal Metrics* application note
- Texas Instruments, *Using New Thermal Metrics* application note
- Texas Instruments, *Thermal Characteristics of Linear and Logic Packages Using JEDEC PCB Designs* application note

9.2 Device Nomenclature

表 9-1. Available Options(1)

PRODUCT	V_{OUT}
LP2985**cxxxz-y.y**/NOPB Legacy chip	**xxx** is the package designator. **z** is the package quantity. X is for large quantity reel and non-X is for small quantity reel. **y.y** is the nominal output voltage (for example, 3.3 = 3.3 V; 5.0 = 5.0 V). **c** is the accuracy specification, **A** for higher accuracy and non-A for standard grade.
LP2985**Axxxz-y.y/M3** New chip	**xxx** is the package designator. **z** is the package quantity. X is for large quantity reel and non-X is for small quantity reel **y.y** is the nominal output voltage (for example, 3.3 = 3.3 V; 5.0 = 5.0 V). **M3** is a suffix designator for newer chip redesigns, fabricated on the latest TI process technology.

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or visit the device product folder at www.ti.com.

9.3 接收文档更新通知

要接收文档更新通知，请导航至 ti.com 上的器件产品文件夹。点击*订阅更新* 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

9.4 支持资源

TI E2E™ 支持论坛是工程师的重要参考资料，可直接从专家获得快速、经过验证的解答和设计帮助。搜索现有解答或提出自己的问题可获得所需的快速设计帮助。

链接的内容由各个贡献者“按原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的《使用条款》。

9.5 Trademarks

TI E2E™ is a trademark of Texas Instruments.
所有商标均为其各自所有者的财产。

9.6 静电放电警告

静电放电 (ESD) 会损坏这个集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

9.7 术语表

TI 术语表　　本术语表列出并解释了术语、首字母缩略词和定义。

10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
LP2985AIM5-2.5/NO.A	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LAUA
LP2985AIM5-2.5/NOPB	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 125	LAUA
LP2985AIM5-2.7/NO.A	Active	Production	SOT-23 (DBV) | 5	1000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	LALA
LP2985AIM5-2.7/NOPB	Active	Production	SOT-23 (DBV) | 5	1000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	LALA
LP2985AIM5-2.8/NO.A	Active	Production	SOT-23 (DBV) | 5	1000 | SMALL T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	L0KA
LP2985AIM5-2.8/NOPB	Active	Production	SOT-23 (DBV) | 5	1000 | SMALL T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	L0KA
LP2985AIM5-2.9/NO.A	Active	Production	SOT-23 (DBV) | 5	1000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	LAXA
LP2985AIM5-2.9/NOPB	Active	Production	SOT-23 (DBV) | 5	1000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	LAXA
LP2985AIM5-3.0/NO.A	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	L0OA
LP2985AIM5-3.0/NOPB	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 125	L0OA
LP2985AIM5-3.1/NO.A	Active	Production	SOT-23 (DBV) | 5	1000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	L0PA
LP2985AIM5-3.1/NOPB	Active	Production	SOT-23 (DBV) | 5	1000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	L0PA
LP2985AIM5-3.3/NO.A	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	L0RA
LP2985AIM5-3.3/NOPB	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	L0RA
LP2985AIM5-3.6/NO.A	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	L0SA
LP2985AIM5-3.6/NOPB	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 125	L0SA
LP2985AIM5-3.8/NO.A	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	L0YA
LP2985AIM5-3.8/NOPB	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 125	L0YA
LP2985AIM5-4.0/NO.A	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	L0TA
LP2985AIM5-4.0/NOPB	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	L0TA
LP2985AIM5-4.5/NO.A	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LA7A
LP2985AIM5-4.5/NOPB	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 125	LA7A
LP2985AIM5-5.0/NO.A	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	L0UA
LP2985AIM5-5.0/NOPB	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	L0UA
LP2985AIM5-5.7/NO.A	Active	Production	SOT-23 (DBV) | 5	1000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	LKTA
LP2985AIM5-5.7/NOPB	Active	Production	SOT-23 (DBV) | 5	1000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-	LKTA
LP2985AIM5-6.1/NO.A	Active	Production	SOT-23 (DBV) | 5	1000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	LF6A
LP2985AIM5-6.1/NOPB	Active	Production	SOT-23 (DBV) | 5	1000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	LF6A
LP2985AIM5X-2.5/NO.A	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LAUA

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
LP2985AIM5X-2.5/NOPB	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 125	LAUA
LP2985AIM5X-2.6/NO.A	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	LCEA
LP2985AIM5X-2.6/NOPB	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	LCEA
LP2985AIM5X-2.8/NO.A	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	L0KA
LP2985AIM5X-2.8/NOPB	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 125	L0KA
LP2985AIM5X-2.9/NO.A	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	LAXA
LP2985AIM5X-2.9/NOPB	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	LAXA
LP2985AIM5X-3.0/NO.A	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	L0OA
LP2985AIM5X-3.0/NOPB	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 125	L0OA
LP2985AIM5X-3.1/NO.A	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	L0PA
LP2985AIM5X-3.1/NOPB	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	L0PA
LP2985AIM5X-3.3/NO.A	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	L0RA
LP2985AIM5X-3.3/NOPB	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	L0RA
LP2985AIM5X-3.6/M3	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	L0SA
LP2985AIM5X-3.6/M3.A	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	L0SA
LP2985AIM5X-3.6/NO.A	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	L0SA
LP2985AIM5X-3.6/NOPB	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 125	L0SA
LP2985AIM5X-3.8/NO.A	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	L0YA
LP2985AIM5X-3.8/NOPB	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	L0YA
LP2985AIM5X-4.0/NO.A	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	L0TA
LP2985AIM5X-4.0/NOPB	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 125	L0TA
LP2985AIM5X-4.5/NO.A	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LA7A
LP2985AIM5X-4.5/NOPB	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 125	LA7A
LP2985AIM5X-5.0/NO.A	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	L0UA
LP2985AIM5X-5.0/NOPB	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 125	L0UA
LP2985AIM5X-6.1/NO.A	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	LF6A
LP2985AIM5X-6.1/NOPB	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	LF6A
LP2985IM5-2.5/NOPB	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 125	LAUB
LP2985IM5-2.5/NOPB.A	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LAUB
LP2985IM5-2.7/NOPB	Active	Production	SOT-23 (DBV) | 5	1000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-	LALB
LP2985IM5-2.7/NOPB.A	Active	Production	SOT-23 (DBV) | 5	1000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	LALB

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
LP2985IM5-2.7/NOPB.B	Active	Production	SOT-23 (DBV) | 5	1000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	LALB
LP2985IM5-2.8/NOPB	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 125	L0KB
LP2985IM5-2.8/NOPB.A	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	L0KB
LP2985IM5-2.9/NOPB	Active	Production	SOT-23 (DBV) | 5	1000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	LAXB
LP2985IM5-2.9/NOPB.A	Active	Production	SOT-23 (DBV) | 5	1000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	LAXB
LP2985IM5-2.9/NOPB.B	Active	Production	SOT-23 (DBV) | 5	1000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	LAXB
LP2985IM5-3.0/NOPB	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 125	L0OB
LP2985IM5-3.0/NOPB.A	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	L0OB
LP2985IM5-3.1/NOPB	Active	Production	SOT-23 (DBV) | 5	1000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	L0PB
LP2985IM5-3.1/NOPB.A	Active	Production	SOT-23 (DBV) | 5	1000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	L0PB
LP2985IM5-3.1/NOPB.B	Active	Production	SOT-23 (DBV) | 5	1000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	L0PB
LP2985IM5-3.2/NOPB	Active	Production	SOT-23 (DBV) | 5	1000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	L0QB
LP2985IM5-3.2/NOPB.A	Active	Production	SOT-23 (DBV) | 5	1000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	L0QB
LP2985IM5-3.2/NOPB.B	Active	Production	SOT-23 (DBV) | 5	1000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	L0QB
LP2985IM5-3.3/NOM3	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	L0RB
LP2985IM5-3.3/NOM3.A	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	L0RB
LP2985IM5-3.3/NOPB	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 125	L0RB
LP2985IM5-3.3/NOPB.A	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	L0RB
LP2985IM5-3.5/NOPB	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 125	LAIB
LP2985IM5-3.5/NOPB.A	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LAIB
LP2985IM5-3.6/NOPB	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 125	(L0SB, L0YB)
LP2985IM5-3.6/NOPB.A	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	(L0SB, L0YB)
LP2985IM5-3.8/NOPB	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 125	L0YB
LP2985IM5-3.8/NOPB.A	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	L0YB
LP2985IM5-4.0/NOPB	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 125	L0TB
LP2985IM5-4.0/NOPB.A	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	L0TB
LP2985IM5-4.5/NOPB	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU | SN	Level-1-260C-UNLIM	-	LA7B
LP2985IM5-4.5/NOPB.A	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LA7B
LP2985IM5-5.0/NOPB	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 125	L0UB
LP2985IM5-5.0/NOPB.A	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	L0UB
LP2985IM5-5.7/NOPB	Active	Production	SOT-23 (DBV) | 5	1000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-	LKTB

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
LP2985IM5-5.7/NOPB.A	Active	Production	SOT-23 (DBV) | 5	1000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	LKTB
LP2985IM5-5.7/NOPB.B	Active	Production	SOT-23 (DBV) | 5	1000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	LKTB
LP2985IM5-6.1/NOPB	Active	Production	SOT-23 (DBV) | 5	1000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-	LF6B
LP2985IM5-6.1/NOPB.A	Active	Production	SOT-23 (DBV) | 5	1000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	LF6B
LP2985IM5-6.1/NOPB.B	Active	Production	SOT-23 (DBV) | 5	1000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	LF6B
LP2985IM5X-2.5/NO.A	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LAUB
LP2985IM5X-2.5/NOPB	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 125	LAUB
LP2985IM5X-2.7/NO.A	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	LALB
LP2985IM5X-2.7/NOPB	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-	LALB
LP2985IM5X-2.8/NO.A	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	L0KB
LP2985IM5X-2.8/NOPB	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 125	L0KB
LP2985IM5X-3.0/NO.A	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	L0OB
LP2985IM5X-3.0/NOPB	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 125	L0OB
LP2985IM5X-3.3/NO.A	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	L0RB
LP2985IM5X-3.3/NOPB	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 125	L0RB
LP2985IM5X-3.6/NO.A	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	L0SB
LP2985IM5X-3.6/NOPB	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	L0SB
LP2985IM5X-4.0/NO.A	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	L0TB
LP2985IM5X-4.0/NOPB	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 125	L0TB
LP2985IM5X-4.5/NO.A	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LA7B
LP2985IM5X-4.5/NOPB	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU | SN	Level-1-260C-UNLIM	-	LA7B
LP2985IM5X-5.0/NO.A	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	L0UB
LP2985IM5X-5.0/NOPB	Active	Production	SOT-23 (DBV) | 5	3000 | LARGE T&R	Yes	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 125	L0UB

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

[4] **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

[5] **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

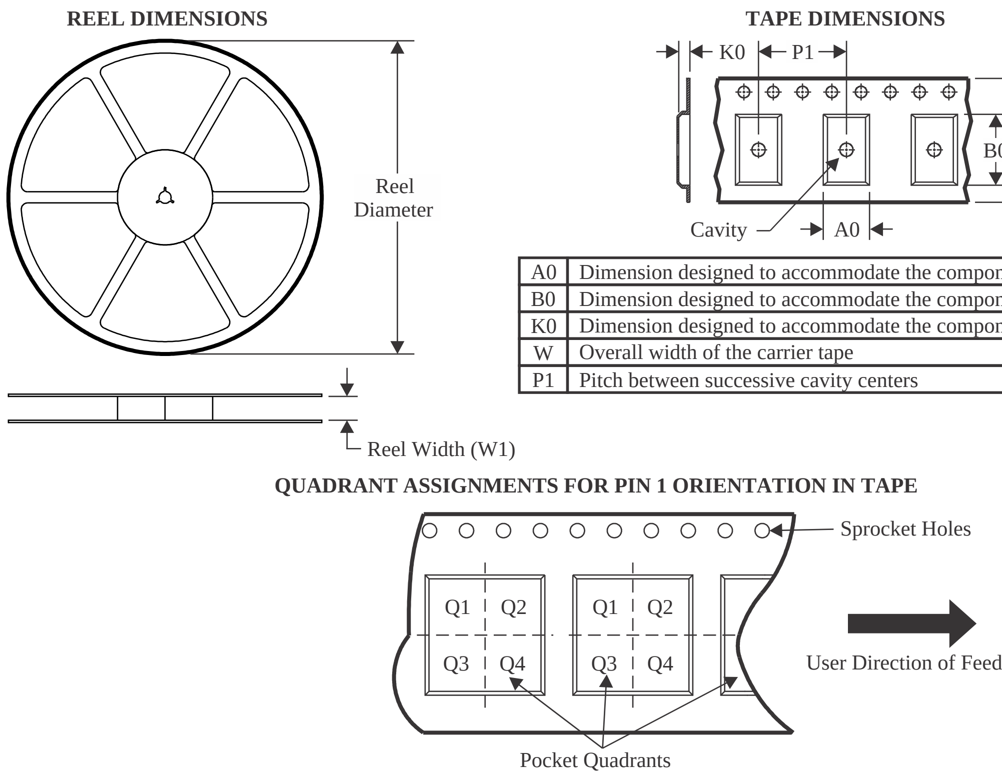
[6] **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION



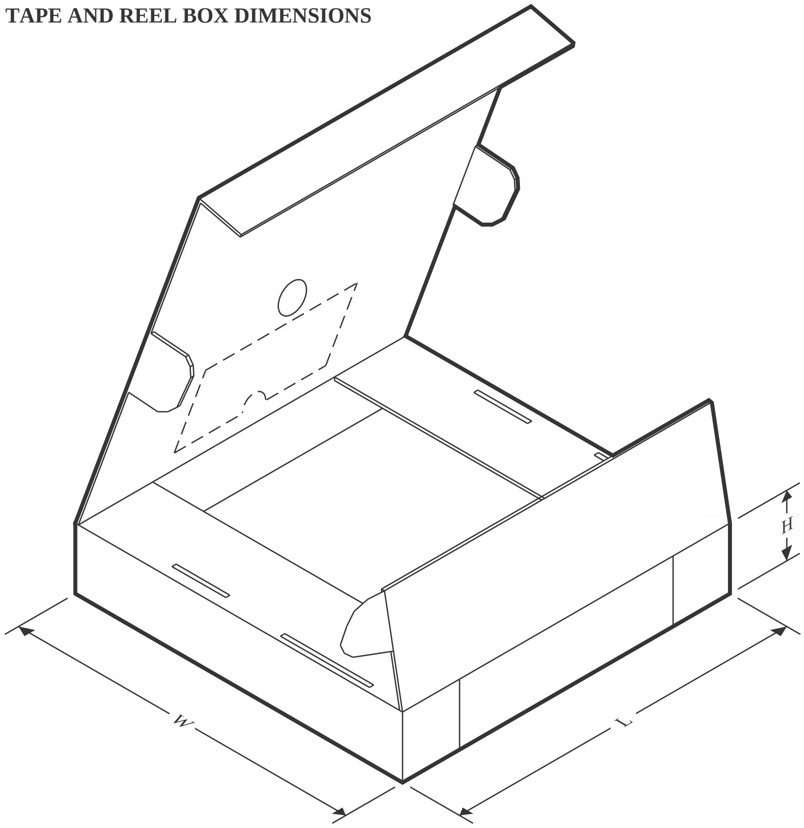
A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LP2985AIM5-2.5/NOPB	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP2985AIM5-2.7/NOPB	SOT-23	DBV	5	1000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP2985AIM5-2.8/NOPB	SOT-23	DBV	5	1000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP2985AIM5-2.9/NOPB	SOT-23	DBV	5	1000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP2985AIM5-3.0/NOPB	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP2985AIM5-3.1/NOPB	SOT-23	DBV	5	1000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP2985AIM5-3.3/NOPB	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP2985AIM5-3.6/NOPB	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP2985AIM5-3.8/NOPB	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP2985AIM5-4.0/NOPB	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP2985AIM5-4.5/NOPB	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP2985AIM5-5.0/NOPB	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP2985AIM5-5.7/NOPB	SOT-23	DBV	5	1000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP2985AIM5-6.1/NOPB	SOT-23	DBV	5	1000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP2985AIM5X-2.5/NOPB	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP2985AIM5X-2.6/NOPB	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LP2985AIM5X-2.8/NOPB	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP2985AIM5X-2.9/NOPB	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP2985AIM5X-3.0/NOPB	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP2985AIM5X-3.1/NOPB	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP2985AIM5X-3.3/NOPB	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP2985AIM5X-3.3/NOPB	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP2985AIM5X-3.6/M3	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP2985AIM5X-3.6/NOPB	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP2985AIM5X-3.8/NOPB	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP2985AIM5X-4.0/NOPB	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP2985AIM5X-4.5/NOPB	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP2985AIM5X-5.0/NOPB	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP2985AIM5X-6.1/NOPB	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP2985IM5-2.5/NOPB	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP2985IM5-2.7/NOPB	SOT-23	DBV	5	1000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP2985IM5-2.8/NOPB	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP2985IM5-2.9/NOPB	SOT-23	DBV	5	1000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP2985IM5-3.0/NOPB	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP2985IM5-3.1/NOPB	SOT-23	DBV	5	1000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP2985IM5-3.2/NOPB	SOT-23	DBV	5	1000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP2985IM5-3.3/NOM3	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP2985IM5-3.3/NOPB	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP2985IM5-3.5/NOPB	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP2985IM5-3.6/NOPB	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP2985IM5-3.8/NOPB	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP2985IM5-4.0/NOPB	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP2985IM5-4.5/NOPB	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP2985IM5-5.0/NOPB	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP2985IM5-5.7/NOPB	SOT-23	DBV	5	1000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP2985IM5-6.1/NOPB	SOT-23	DBV	5	1000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP2985IM5X-2.5/NOPB	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP2985IM5X-2.7/NOPB	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP2985IM5X-2.8/NOPB	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP2985IM5X-3.0/NOPB	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP2985IM5X-3.3/NOPB	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP2985IM5X-3.6/NOPB	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP2985IM5X-4.0/NOPB	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP2985IM5X-4.5/NOPB	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LP2985IM5X-5.0/NOPB	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3

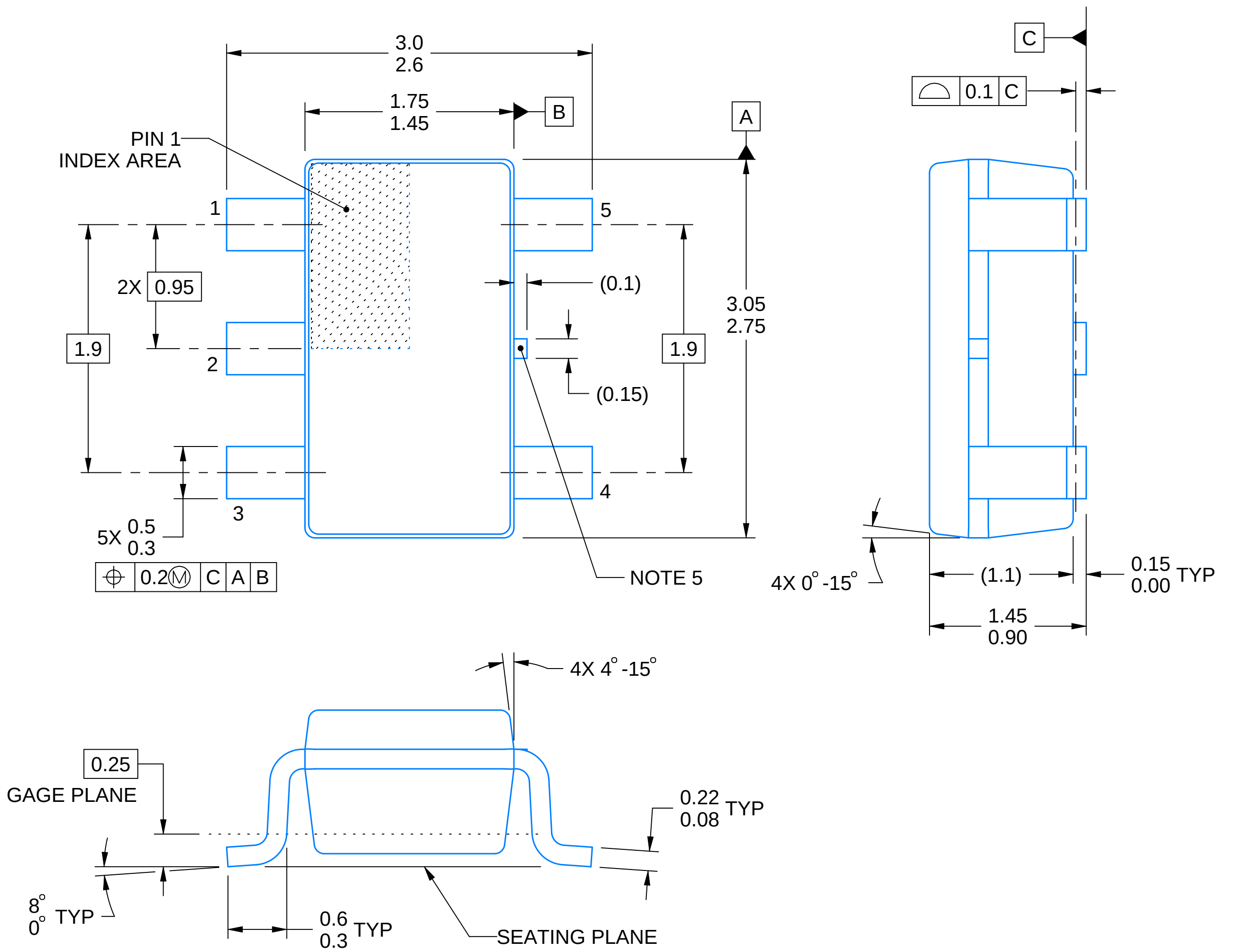
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LP2985AIM5-2.5/NOPB	SOT-23	DBV	5	3000	208.0	191.0	35.0
LP2985AIM5-2.7/NOPB	SOT-23	DBV	5	1000	208.0	191.0	35.0
LP2985AIM5-2.8/NOPB	SOT-23	DBV	5	1000	208.0	191.0	35.0
LP2985AIM5-2.9/NOPB	SOT-23	DBV	5	1000	208.0	191.0	35.0
LP2985AIM5-3.0/NOPB	SOT-23	DBV	5	3000	208.0	191.0	35.0
LP2985AIM5-3.1/NOPB	SOT-23	DBV	5	1000	208.0	191.0	35.0
LP2985AIM5-3.3/NOPB	SOT-23	DBV	5	3000	210.0	185.0	35.0
LP2985AIM5-3.6/NOPB	SOT-23	DBV	5	3000	210.0	185.0	35.0
LP2985AIM5-3.8/NOPB	SOT-23	DBV	5	3000	210.0	185.0	35.0
LP2985AIM5-4.0/NOPB	SOT-23	DBV	5	3000	210.0	185.0	35.0
LP2985AIM5-4.5/NOPB	SOT-23	DBV	5	3000	210.0	185.0	35.0
LP2985AIM5-5.0/NOPB	SOT-23	DBV	5	3000	208.0	191.0	35.0
LP2985AIM5-5.7/NOPB	SOT-23	DBV	5	1000	208.0	191.0	35.0
LP2985AIM5-6.1/NOPB	SOT-23	DBV	5	1000	208.0	191.0	35.0
LP2985AIM5X-2.5/NOPB	SOT-23	DBV	5	3000	208.0	191.0	35.0
LP2985AIM5X-2.6/NOPB	SOT-23	DBV	5	3000	208.0	191.0	35.0
LP2985AIM5X-2.8/NOPB	SOT-23	DBV	5	3000	208.0	191.0	35.0
LP2985AIM5X-2.9/NOPB	SOT-23	DBV	5	3000	208.0	191.0	35.0

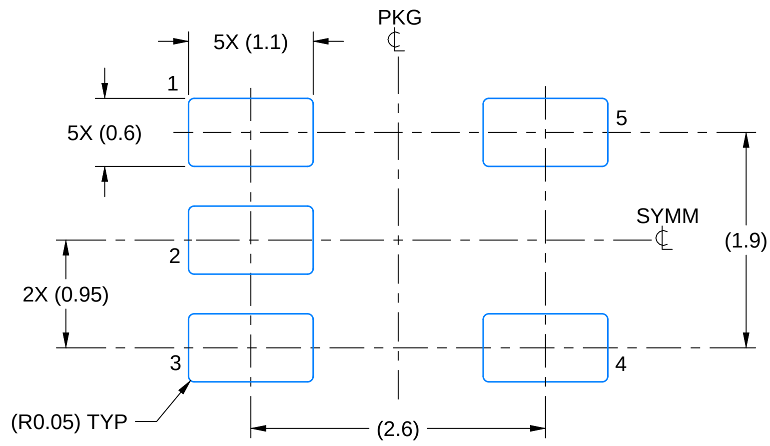
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LP2985AIM5X-3.0/NOPB	SOT-23	DBV	5	3000	208.0	191.0	35.0
LP2985AIM5X-3.1/NOPB	SOT-23	DBV	5	3000	208.0	191.0	35.0
LP2985AIM5X-3.3/NOPB	SOT-23	DBV	5	3000	210.0	185.0	35.0
LP2985AIM5X-3.3/NOPB	SOT-23	DBV	5	3000	210.0	185.0	35.0
LP2985AIM5X-3.6/M3	SOT-23	DBV	5	3000	210.0	185.0	35.0
LP2985AIM5X-3.6/NOPB	SOT-23	DBV	5	3000	208.0	191.0	35.0
LP2985AIM5X-3.8/NOPB	SOT-23	DBV	5	3000	208.0	191.0	35.0
LP2985AIM5X-4.0/NOPB	SOT-23	DBV	5	3000	208.0	191.0	35.0
LP2985AIM5X-4.5/NOPB	SOT-23	DBV	5	3000	208.0	191.0	35.0
LP2985AIM5X-5.0/NOPB	SOT-23	DBV	5	3000	210.0	185.0	35.0
LP2985AIM5X-6.1/NOPB	SOT-23	DBV	5	3000	208.0	191.0	35.0
LP2985IM5-2.5/NOPB	SOT-23	DBV	5	3000	208.0	191.0	35.0
LP2985IM5-2.7/NOPB	SOT-23	DBV	5	1000	208.0	191.0	35.0
LP2985IM5-2.8/NOPB	SOT-23	DBV	5	3000	208.0	191.0	35.0
LP2985IM5-2.9/NOPB	SOT-23	DBV	5	1000	208.0	191.0	35.0
LP2985IM5-3.0/NOPB	SOT-23	DBV	5	3000	208.0	191.0	35.0
LP2985IM5-3.1/NOPB	SOT-23	DBV	5	1000	208.0	191.0	35.0
LP2985IM5-3.2/NOPB	SOT-23	DBV	5	1000	208.0	191.0	35.0
LP2985IM5-3.3/NOM3	SOT-23	DBV	5	3000	210.0	185.0	35.0
LP2985IM5-3.3/NOPB	SOT-23	DBV	5	3000	208.0	191.0	35.0
LP2985IM5-3.5/NOPB	SOT-23	DBV	5	3000	208.0	191.0	35.0
LP2985IM5-3.6/NOPB	SOT-23	DBV	5	3000	208.0	191.0	35.0
LP2985IM5-3.8/NOPB	SOT-23	DBV	5	3000	208.0	191.0	35.0
LP2985IM5-4.0/NOPB	SOT-23	DBV	5	3000	210.0	185.0	35.0
LP2985IM5-4.5/NOPB	SOT-23	DBV	5	3000	208.0	191.0	35.0
LP2985IM5-5.0/NOPB	SOT-23	DBV	5	3000	208.0	191.0	35.0
LP2985IM5-5.7/NOPB	SOT-23	DBV	5	1000	208.0	191.0	35.0
LP2985IM5-6.1/NOPB	SOT-23	DBV	5	1000	208.0	191.0	35.0
LP2985IM5X-2.5/NOPB	SOT-23	DBV	5	3000	208.0	191.0	35.0
LP2985IM5X-2.7/NOPB	SOT-23	DBV	5	3000	208.0	191.0	35.0
LP2985IM5X-2.8/NOPB	SOT-23	DBV	5	3000	210.0	185.0	35.0
LP2985IM5X-3.0/NOPB	SOT-23	DBV	5	3000	208.0	191.0	35.0
LP2985IM5X-3.3/NOPB	SOT-23	DBV	5	3000	208.0	191.0	35.0
LP2985IM5X-3.6/NOPB	SOT-23	DBV	5	3000	208.0	191.0	35.0
LP2985IM5X-4.0/NOPB	SOT-23	DBV	5	3000	208.0	191.0	35.0
LP2985IM5X-4.5/NOPB	SOT-23	DBV	5	3000	208.0	191.0	35.0
LP2985IM5X-5.0/NOPB	SOT-23	DBV	5	3000	208.0	191.0	35.0



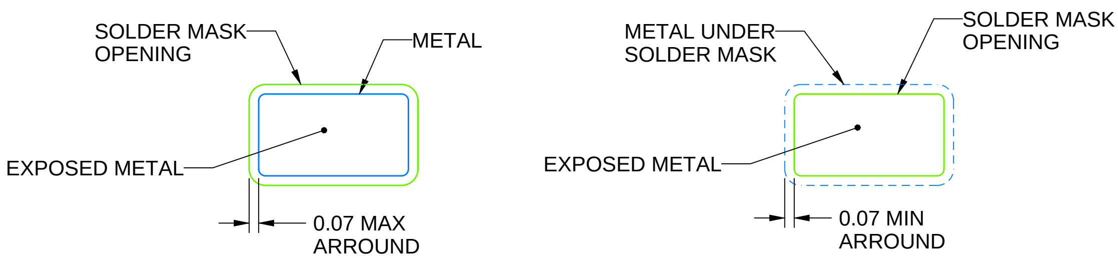
4214839/K 08/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-178.
4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25 mm per side.
5. Support pin may differ or may not be present.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X



NON SOLDER MASK
DEFINED
(PREFERRED)

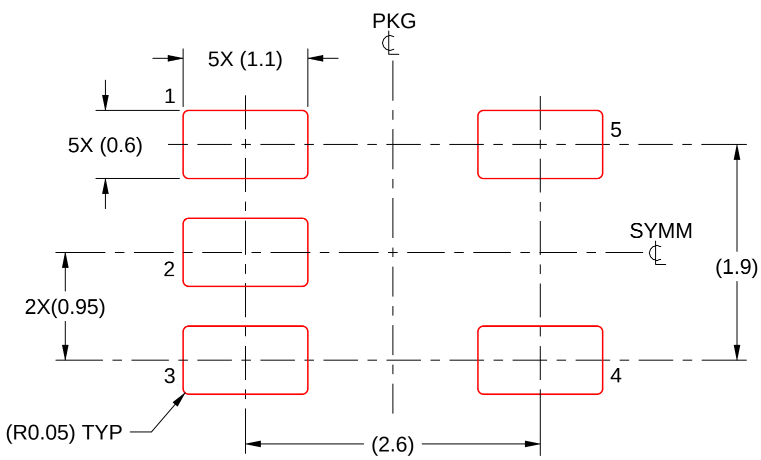
SOLDER MASK
DEFINED

SOLDER MASK DETAILS

4214839/K 08/2024

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4214839/K 08/2024

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

重要通知和免责声明

TI“按原样”提供技术和可靠性数据（包括数据表）、设计资源（包括参考设计）、应用或其他设计建议、网络工具、安全信息和其他资源，不保证没有瑕疵且不做出任何明示或暗示的担保，包括但不限于对适销性、某特定用途方面的适用性或不侵犯任何第三方知识产权的暗示担保。

这些资源可供使用 TI 产品进行设计的熟练开发人员使用。您将自行承担以下全部责任：(1) 针对您的应用选择合适的 TI 产品，(2) 设计、验证并测试您的应用，(3) 确保您的应用满足相应标准以及任何其他功能安全、信息安全、监管或其他要求。

这些资源如有变更，恕不另行通知。TI 授权您仅可将这些资源用于研发本资源所述的 TI 产品的相关应用。 严禁以其他方式对这些资源进行复制或展示。您无权使用任何其他 TI 知识产权或任何第三方知识产权。您应全额赔偿因在这些资源的使用中对 TI 及其代表造成的任何索赔、损害、成本、损失和债务，TI 对此概不负责。

TI 提供的产品受 TI 的销售条款或 ti.com 上其他适用条款/TI 产品随附的其他适用条款的约束。TI 提供这些资源并不会扩展或以其他方式更改 TI 针对 TI 产品发布的适用的担保或担保免责声明。

TI 反对并拒绝您可能提出的任何其他或不同的条款。

邮寄地址：Texas Instruments, Post Office Box 655303, Dallas, Texas 75265